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Efficient optimization of integrated spiral inductor with bounding of layout design parameters

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Abstract In this paper we present an efficient method of determining the optimized layout of on chip spiral inductor. The method initially identifies the feasible region of optimization by developing layout design parameter bound curves for a large range of physical inductance values that satisfies the same area specification. For any desired inductance value the upper and lower bounds of the optimization variables are determined graphically. An enumeration algorithm implemented finds the global optimum layout that gives the highest quality factor in less than 1 s of CPU time with less function evaluations. The optimization method also gives the performance of all possible combinations that results the same inductance value. Subsequently important fundamental tradeoff of the design like quality factor and area, quality factor and inductance, quality factor and operating frequency, maximum quality factor and the peak frequency is explored in few seconds. The method also gives other valuable information such as sensitivity of the inductance and quality factor to the layout design parameters. The accuracy of the proposed method is verified using a 3D electromagnetic simulator.

Keywords Spiral inductor · Optimization · Quality factor · RFIC · Passive circuits

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1 Introduction

The expansion of wireless communication market has increased the demand for small size, low cost and high performance radio frequency integrated circuits (RFIC's). Steady improvements in the radio frequency (RF) characteristics of Complementary Metal Oxide Semiconductor (CMOS) devices via scaling driven by advancement in lithography, has enabled increased integration of RF functions and hence CMOS technology has been widely adopted for its mature and mass productivity [1, 2]. The performance of CMOS RFIC's such as voltage controlled oscillators (VCO's), low noise amplifiers (LNA's), passive element filters etc. are well determined by the quality of the passive components, of which inductors are the most critical [3]. For example, the quality factor of the inductor determines the stability and phase-noise power of an oscillator for any communication applications and the ability to implement extremely selective filters with small percent bandwidth, small shape factor and low insertion loss.

The figure of merit (FOM) of on chip spiral inductors are (i) quality factor, Q (ii) optimum frequency, f_{max} at which Q reaches its maximum value, Q_{max} and (iii) self-resonance frequency, f_{res} at which the inductor behaves like a parallel RC circuit in resonance and is far from behaving as an inductor [1]. These properties of the spiral inductor are determined by its geometrical or layout parameters and the technological parameters. The layout parameters are sketched in Fig. 1, which includes the number of turns (N), spiral track width (W), spiral track spacing (S), outer diameter (D_{out}) and inner diameter (D_{in}). The technological parameters are substrate resistivity, insulator thickness, conductor thickness and resistance. The dependence of the quality factor and inductance on these parameters has been studied [4–7]. In [7] the performance trend with the layout

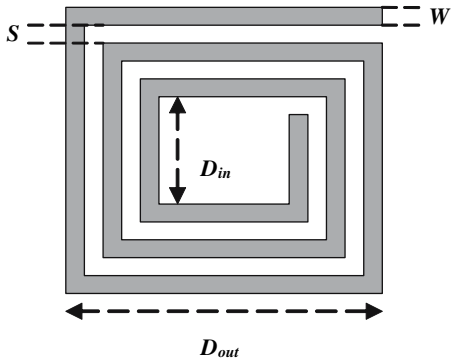

Fig. 1 Layout of a square spiral inductor

parameters was studied keeping the inductance value constant. On-chip spiral inductors fabricated on Silicon substrate suffers from poor quality factor due to ohmic and substrate losses. The quality factor is inversely proportional to the finite resistance of the metal layer which becomes a complex function at high frequencies and the losses in inductor increases as a result of induced currents and dielectric loss. The low resistivity of silicon substrate also results in capacitive and inductive coupling to the substrate. For a given technology, the material and process parameters are fixed and only the layout parameters are available for variation. These losses, then must be minimized by a careful design and optimization of the layout parameters.

Inductors are generally designed either based on a library of previously available fabricated inductors or using an electromagnetic simulator. The former method limits the design space and the later is computationally expensive and time consuming. A typical spiral inductor design problem involves (i) the design phase i.e., determine all possible combinations of the layout parameters such as N, W, D_{out} or D_{in} and S that results the desired inductance value and (ii) the optimization phase i.e., identify the combination that will result the highest quality factor at desired frequency with a high self resonance frequency, f_{res}. Thus, the complexity in the design of an on chip inductor lies in deciding these layout parameters in order to achieve the target inductance with its desired quality factor. An efficient method to determine the optimum layout parameters is the utmost need for an RFIC designer to shorten the design and product time-to-market cycle.

Various methods have been proposed to design and optimize an inductor. In enumeration methods like [8, 9] the design parameters are first discretized and each combination is simulated to obtain a performance metric value. The design resulting the best performance metric value is considered optimal. This method is simple and can find a nearly global optimum design but it is highly inefficient. Numerical optimization techniques based on geometric programming [10, 11], sequential quadratic programming [12, 13], simulated annealing [14], artificial neural network [15] has proved to be more efficient reducing the computation time and converging rapidly to the optimal design. In all numerical algorithms the primary goal function is to maximize the quality factor subject to a required inductance value and other design specifications. The results of such algorithms gives a single set of inductor design parameters and no information is available on how far the other combinations are from the optimal one. Information of near optimal solution is also important to judiciously explore the tradeoff between the different competing figure of merits. On the other hand the design parameter constraints always includes sets of infeasible specifications which will increase the number of function evaluations and computation time. The limits on the bounds of the optimization constraints must be cautiously selected to restrict the search space and promote fast convergence to a solution.

The inductance value of a spiral inductor is mainly decided by its geometrical layout parameters [5]. The bounding on the layout parameters is important to speed up the optimum inductor synthesis. In this paper we present a simple algorithm to decide the bounds on the design parameters of spiral inductor for a large range of physical inductance values that satisfies a given area specification. With this parameter bounds we can eliminate a large proportion of the redundant sample designs. In this way the feasible region of the optimization problem is carefully determined. Hence the number of function evaluations required to converge to the optimum solution is reduced and the efficiency of optimization is improved. The paper is organized as follows. In Sect. 2, the proposed method to decide the bounds of design parameters for any specified value of inductance is explained. The proposed method is implemented with an enumeration algorithm in Sect. 3 and the advantage is illustrated by the results in Sect. 4. Finally conclusions are drawn in Sect. 5.

2 Bounding of layout parameters

A spiral inductor optimization problem may be formulated as

$$\begin{array}{ll} \text{maximize} & Q\,(N,W,D,S) \\ \text{subject to} & L(N,W,D,S) \le L_{\text{desired}} \\ & N_{\min} \le N \le N_{\max} \\ & W_{\min} \le W \le W_{\max} \\ & S_{\min} \le S \le S_{\max} \\ & D_{\min} \le D \le D_{\max} \end{array}$$

where $Q\,(N,W,D,S)$ is the objective function and N, W, D and S are the optimization variables. The set of sample points for which the objective function and all constraints

are defined is the domain of the optimization problem and the set of all points that satisfies all the constraints is the feasible set. The size of the design search space and number of function evaluation will be determined by the lower and upper bounds on these variables. For fewer function evaluation it is important to restrict the search space only to the feasible region. This means that only the range of N, W, D and S which will result in the desired value of inductance must be specified to the optimizer. In this section we demonstrate a method of bounding on these optimization variables and locate the feasible region for any desired value of inductance.

The spiral inductor design variables N, W, D and S are not independent. The limits on the outer diameter will decide the possible combinations of N, W and S governed by the relation

$$D_{\text{out}} = D_{\text{in}} + 2\,W\,N + 2\,S\,(N-1) \tag{1}$$

Therefore to simplify, we assume that the spiral inductor outer diameter is specified. For any desired inductance value several combination of the N, W, D_{out} or D_{in} and S exist. Also there will be certainly a range of inductance values that satisfies the same area limitation. The algorithm develops the spiral inductor layout parameter bound curves of all such inductors and these curves can then be used to determine the bound on number of turns and width for any value of inductance that can be designed satisfying the same area limitation. The algorithm is explained by the flowchart in Fig. 2 and it consists of three major steps as given below:

(i) Determine the maximum number of turns, $N_{\max}$ that can be accommodated in the limited area for each width and spacing of the spiral.
(ii) Keep the outer diameter, D_{out} at maximum and constant. For each width, W and S, vary the number of turns from 1 to $N_{\max}$, keeping $D_{\text{in}} \geq D_{\text{in, min}}$ and compute the inductance for each case. One may consider that the turns of the inductor are spiraling in gradually. Therefore, in each combination D_{in} will vary and will be at its maximum limit for each N, W and S combination.
(iii) Keep the inner diameter, D_{in} minimum and constant. For each width and spacing, vary the number of turns from 1 to $N_{\max}$, keeping $D_{\text{out}} \leq D_{\text{out, max}}$ and compute the inductance for each case again. Here we may consider that the turns of the inductor are spiraling out gradually. Similarly, D_{out} will vary for each N, W and S combination within the area limit.

The inner or outer diameter is given by Eq. 1. In this way, for each N, W and S combination we will get the maximum inductance from step (ii) and minimum inductance from step (iii) by varying D_{in} and D_{out} within the area limits. The inductance is calculated using the algorithm developed by Greenhouse [16] based on Grover's formula where the planar spiral is divided into a number of straight conductor segments; the total inductance is calculated as the sum of all the self-inductance of the straight segments and mutual inductance, both positive and negative between the parallel segments.

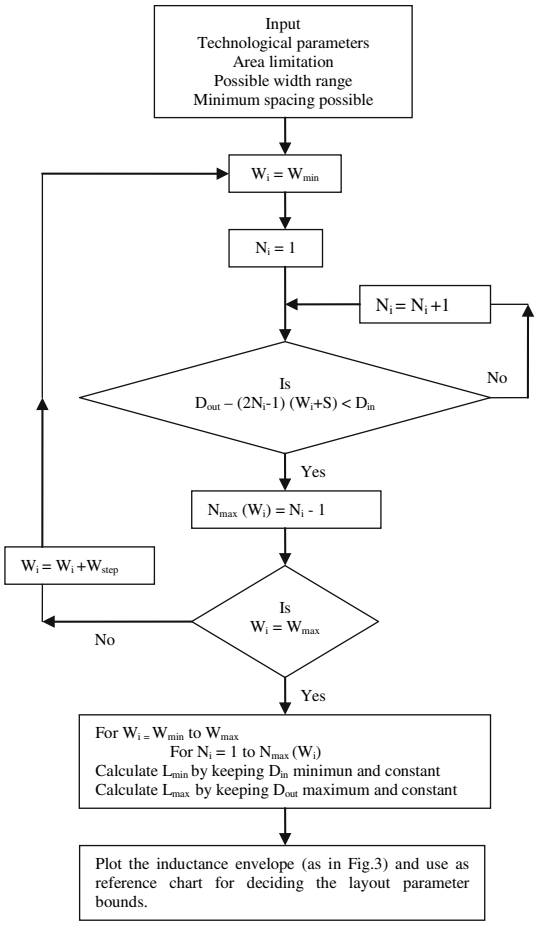

Fig. 2 Flowchart to determine the layout parameter bounds of spiral inductor

To illustrate the methodology we consider here an example, where D_{out} is assumed to be 400 μm. The width was chosen to vary from 5 μm to 25 μm. Several studies [4, 7, 17] has shown that tight coupling of the magnetic field maximizes the quality factor and reduces the chip area for a given inductor layout. The interwinding capacitance from tighter coupling has only a slight impact on performance . Therefore the spacing was kept constant at 2 μm. The largest $N_{\max}$ was found to be 26. The possible inductances varies from 0.13 nH to 140 nH. The minimum and maximum inductance of all possible combination of N, W and S is shown in Figs. 3 and 4, respectively. In the figure,

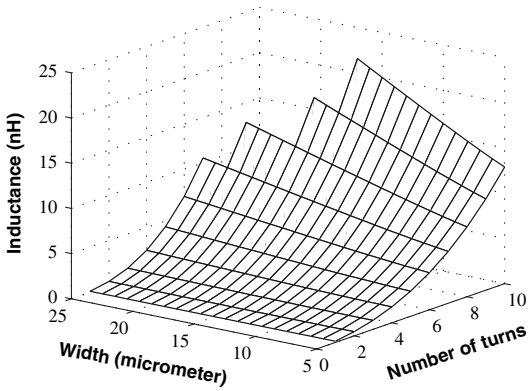

Fig. 3 Minimum inductance for all combinations of N = 1–10 and W = 5–25 μm within the area 400 μm × 400 μm. Spacing fixed at 2 μm

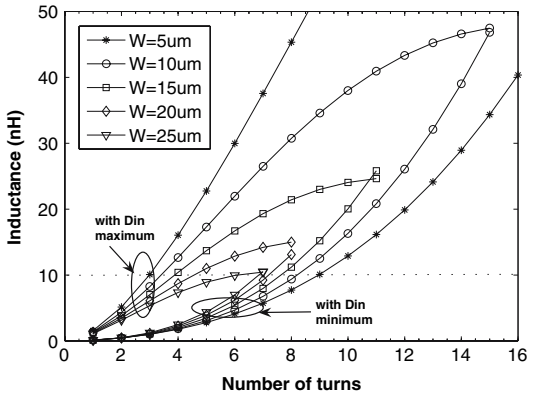

Fig. 5 Layout parameter bound curves of possible inductances by varying D_{in} from minimum to maximum for all combination of number of turns and width that satisfies the area 400 μm × 400 μm. Spacing fixed at 2 μm

inductance values only for number of turns up to 10 are shown and D_{in} was allowed to be as small as 50 μm. The information from Figs. 3 and 4 is combined to generate the layout parameter bound curves as shown in Fig. 5. The curves are plotted only for width 5 μm, 10 μm, 15 μm, 20 μm, and 25 μm for clarity. The other widths are not shown in the figure but they follow the same pattern. In the figure two groups of curves are shown, one for D_{in} maximum and other one for D_{in} minimum. Here it must be noted that maximum inner diameter D_{in} is different for all widths. Consider the width, W = 25 μm. We can see that the curve with minimum and maximum inner diameter D_{in} meets at N = 7. The region enclosed by these two curve cover all possible inductance that can be designed with W = 25 μm. It can be seen that the inductance varies from 1 nH to 10.5 nH and N varies from 1 to 7 with D_{in} = 52 μm to 375 μm. Similarly, for other widths the region enclosed by the plot with D_{in} maximum and minimum gives the possible inductance that can be designed with each width and the range of turns. Since the graph is shown only for inductance up to 50 nH the intersection point of the plot for W = 5 μm is not seen.

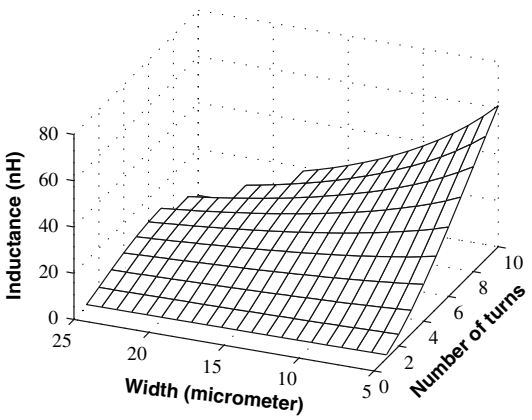

Fig. 4 Maximum inductance for all combinations of N = 1–10 and W = 5–25 μm within the area 400 μm × 400 μm. Spacing fixed at 2 μm

A typical problem is to design a fixed inductance. Let us consider that the desired inductance is 10 nH, so we may draw a straight horizontal line of 10 nH. The line cuts the curves of all widths and the corresponding minimum number of turns is 3 and maximum is 9. Moreover, widths W > 25 μm will not be able to satisfy the area limit and result 10 nH inductance. If W > 25 μm is to be chosen to realize 10 nH then the area has to be increased. Each point in the graph corresponds to different inner diameter. Here D_{in} ranges from 52 μm to 275 μm. Similarly, for L greater than 16 nH, width must be less than 20 μm to satisfy the area limit. In this way we can find the bounds on the width and turns for any inductance and the corresponding inner or outer diameter limits is also determined. Hence the feasible region of the optimization is identified and the optimum search can be performed within the feasible region only. If we consider the spiral area greater than 400 μm × 400 μm, the size of the envelope will increase as maximum number of turns, N_{max} for each width will increase. Similarly, if the spiral area is less than 400 μm × 400 μm, the envelope size will decrease. Therefore the bounding curves must be plotted for the maximum inductor area specified. Even for a different area specification the replotting of the curves would take only few seconds.

The graphical information can be summarized as: (i) For a specified area the range of inductance values that can be realized by each combination of turn, N and width W is obtained. (ii) For any desired value of inductance, the bounds on the number of turns, width and diameter is obtained. In this way, the bounds on the design parameters can be determined and the optimal search can be enhanced. Since the bounding of the design parameters for a large range of inductance values can be done simultaneously, it

will shorten the design cycle especially for applications that require multiple inductors of different values.

3 Optimization based on bounding of parameters

To illustrate that the design time and accuracy of a spiral inductor optimization schedule is improved using the bounding curves we have implemented an enumeration type optimization algorithm similar to [9] and the lower and upper bounds on the constraints of the design parameters is given according to the bounding curves. Since, only the possible combinations of width and number of turns that will result the desired value of inductance is given, the step to check whether design exist is not required as in [9]. The steps of the optimization algorithm is summarized below:

(i) Input the design specifications, such as the desired inductance value, technology parameters and specified operating frequency.
(ii) For $L = L_{\text{desired}}$ refer the layout parameter bounds diagram and read the range of the number of turns and width that will result the exact value of desired inductance. Assign $N = N_{\min}$ to $N_{\max}$ and $W = W_{\min}$ to $W_{\max}$.
(iii) For each N and W combination adjust the inner diameter, D_{in} is so that $L = L_{\text{desired}}$ and calculate the total length of the spiral.
(iv) Compute the quality factor for each combination of turns and width at the desired operating frequency using the lumped element model [18] and store it.
(v) The maximum quality factor $Q_{\max}$ is the optimum solution and its corresponding layout parameters are the optimum layout parameters.
(vi) Verify the design using a 3D electromagnetic simulator.

The optimization is based on the well accepted accurate physical model [18] shown in Fig. 6. L_s, R_s and C_s represent the series inductance, the metal series resistance and the capacitive coupling respectively. C_p and R_p represents the overall parasitic effect of oxide and Si substrate. Quality factor is proportional to the magnetic energy stored which is equal to the difference between the peak magnetic energy and electric energy. Based on this definition Q is calculated as

$$Q = \frac{\omega L_s}{R_s}\frac{R_p}{R_p+[(\frac{\omega L_s}{R_s})^2+1]R_s} \times[1-\frac{R_s^2(C_s+C_p)}{L_s}-\omega^2 L_s(C_s+C_p)] \quad (2)$$

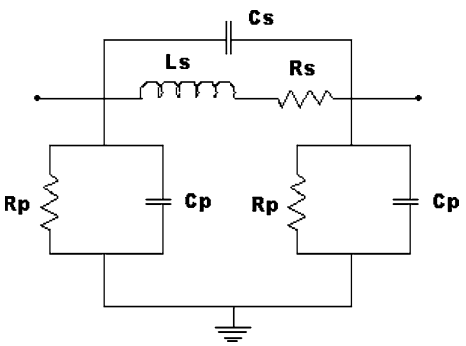

Fig. 6 Simplified lumped element model of on-chip spiral inductor on silicon

4 Results and discussion

In this section we demonstrate the optimization methodology by taking up a problem to optimize the design of 6 nH inductor at 2 GHz. The design constraints and the technology parameters are given in Tables 1 and 2, respectively. A tolerance of 2% is allowed on the inductance value. For an inductance of 6 nH, from the bound curves in Fig. 5 (Sect. 2), we determine the upper and lower bounds on the number of turns and width. The number of turns can vary from 3 to 7 for W varying from 5 μm to 25 μm. The quality factors at 2 GHz as a function of varying width and turns are plotted in Fig. 7 and the corresponding outer diameter is shown in Fig. 8. The highest value of Q is 7.13 for W = 12 μm and N = 4.5 and is marked by a circle. The inner diameter (D_{in}) is 133 μm and outer diameter (D_{out}) is 255 μm. We verified the predicted inductance and the quality factor using a 3D electromagnetic simulator [19]. The frequency dependence of inductance and quality factor for this optimum design are plotted in Figs. 9 and 10, respectively. The inductance calculated using Greenhouse method [16] is 5.92 nH but however at 2 GHz from Fig. 9 the effective inductance is 6.34 nH. There is an error of 6.62 % only. In general inductors are used only in its inductive region i.e., the

Table 1 Optimization constraints

Parameter	Values
Desired inductance	6 nH
Operating frequency	2 GHz
Outer diameter	≤ 400 μm

Table 2 Technological parameters

Parameter	Values
Substrate resistivity	10 Ω cm
Silicon dielectric constant	11.9
Oxide thickness	4.5 μm
Oxide dielectric constant	4
Conductivity of the metal	$5.8 \times 10^5 (\Omega\ \text{cm})^{-1}$
Metal thickness	1 μm

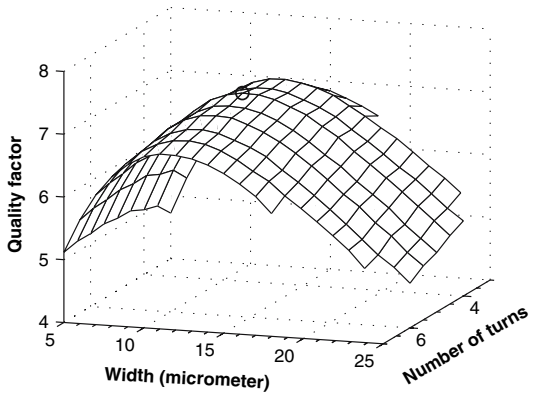

Fig. 7 Quality factors for 6 nH inductors as a function of width and number of turns

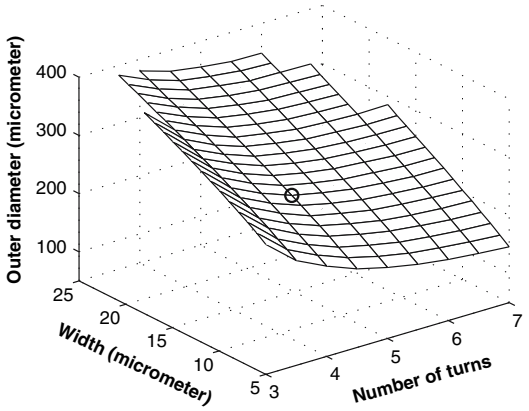

Fig. 8 Outer diameters for 6 nH inductors as a function of width and number of turns

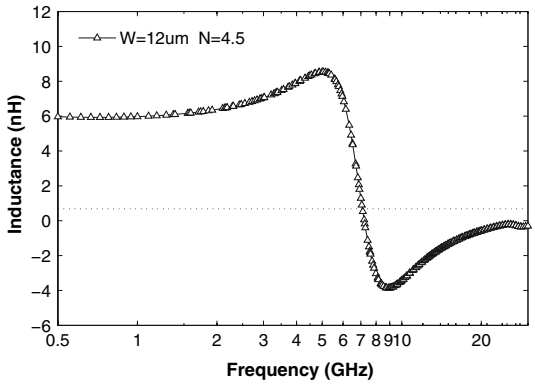

Fig. 9 Inductance of the optimum design of 6 nH inductor as a function of frequency

useful band of operation of an integrated inductor [5] where the inductance value remains relatively constant.

Spiral inductors consume a lot of die area in RF circuitry as compared to the area required by active devices. To minimize the cost, the performance can be carefully traded

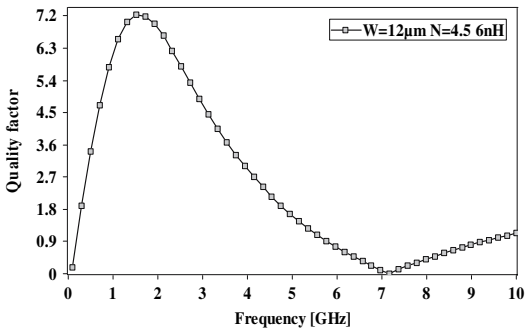

Fig. 10 Quality factor of the optimum design of 6 nH inductor as a function of frequency

off with the area ($D_{out} \times D_{out}$). These tradeoff can also be explored from Figs. 7 and 8. Inductors with larger number of turns has smaller area but quality factor is lower because of smaller inner diameter. The magnetic fields of the adjacent outer turns will pass through some of the innermost turns, inducing eddy current loops which result in non uniform current in the innermost turns thereby increasing the effective resistance and hence lowering the quality factor. This eddy current effect can be minimized by increasing the inner diameter and realized the same inductance with 2–3 turns, but the area will also increase. However, it does not improve quality factor due to the increase in the series resistance as the total length increases with increase in area. For a fixed turn the spiral area also increases with the increase in width. Spiral structure may be selected considering both the quality factor and area. For a 5% reduction in the quality factor, area can be saved by 39% as compared to the optimum structure with the combination $W = 9$ μm, $N = 6$ and $D_{out} = 199$ μm that results $Q = 6.7$. Similarly for a 10% reduction in the quality factor, area can be saved by 49% as compared to the optimum structure with the combination $W = 8$ μm, $N = 7$ and $D_{out} = 181$ μm which results $Q = 6.4$.

In the literature spiral inductor optimization techniques are presented for different process parameters at different operating frequency. So it would be difficult to compare the results closely. For a fair comparison we repeat our optimization with the process parameter in [10, 12, 13]. We have given the result of proposed method and other optimization techniques for inductance values close to 6 nH in Table 3. Enumeration method always results in a global optimum solution as compared to numerical algorithms that may sometimes lead to non convergence and local optimum solutions. We have repeated the optimization to generate the global optimal tradeoff curves for inductance range 1 nH–20 nH at 1 Ghz, 2.4 GHz and 5 GHz and it is shown in Fig. 11. The trend of variation of the corresponding optimum width, number of turns and outer diameter are plotted in Figs. 12–14, respectively. We can

Table 3 Performance comparison of optimization techniques

Methods	L (nH)	Process parameters			S (μm)	*freq* (GHz)	Q_{max}	Optimized layout			Run time (s)
		t_{ox} (μm)	t_{metal} (μm)					W (μm)	N	D_{out} (μm)	
Hershenson [10]	6	5.2	0.9	$\sigma_M = 3 \times 10^5$	1.9	2.5	4	7.8	4.75	206.3	≤ 1
	6	5.2	0.9	$\sigma_M = 3 \times 10^5$ with PGS	1.9	1.5	4.2	13	3.75	292.2	
Zhan [12]	5.7	5	1	$R_{sheet} = 20$	2	2	10.78	17.5	3	400	41
Nieuwoudt [13]	6	6	0.5	$\sigma_M = 5.8 \times 10^5$, $\sigma_{sub} = 7000$	0.5	0.9	3.55	27.26	4.45	367.5	≅ 14
Proposed	6	5.2	0.9	$\sigma_M = 3 \times 10^5$, $\sigma_{sub} = 10$	1.9	2.5	5.21	13	3.5	308	0.219
	6	6	0.5	$\sigma_M = 5.8 \times 10^5$, $\sigma_{sub} = 7000$	0.5	0.9	4.60	30	3.5	432	
	6	4.5	1	$\sigma_M = 5.8 \times 10^5$, $\sigma_{sub} = 10$	2	2	7.13	12	4.5	255	

σ_M : Conductivity of the metal $(\Omega\ cm)^{-1}$

PGS : Protective ground sheild

σ_{sub} : Conductivity of the substrate $(\Omega\ m)^{-1}$

R_{sheet} : Sheet resistance of the metal (m $\Omega/\square$)

see that optimum width decreases with inductance while the number of turns increases in all the three cases. Also for any inductance, as the frequency increases the optimum width decreases and the number of turns increases.

For any inductance, the peak quality factor increases with the increase in frequency as we vary the layout parameters until it reaches its maximum peak quality factor, Q_{max} and the corresponding frequency is referred as f_{max}. Beyond this frequency where the highest value of quality factor is obtained, the peak quality factor will begin to decrease as we change the layout parameters. There also exist a trade off of the maximum quality factor, Q_{max} and the frequency at which it occurs, f_{max}. So we have optimized the quality factor without the frequency constraint to find Q_{max} and f_{max} for inductance range 1 nH–20 nH. The result is shown in Fig. 15. The optimum combination of N, W and D_{out} is given in Table 4. The results presented in

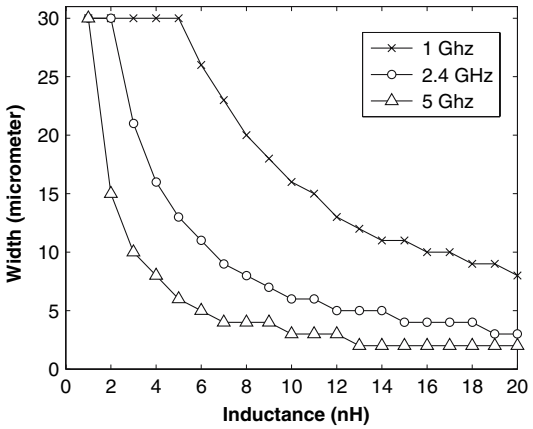

Fig. 12 Optimum width versus inductance at 1 GHz, 2.4 GHz and 5 GHz

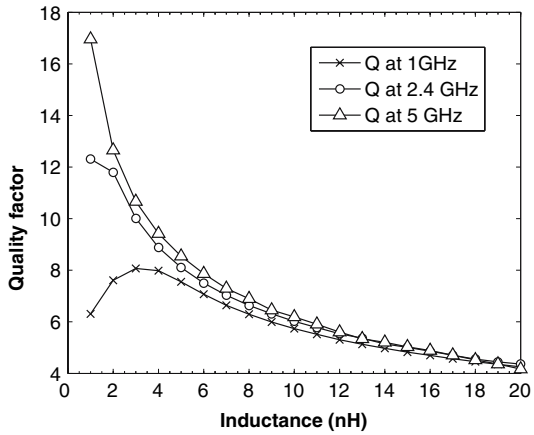

Fig. 11 Global optimal quality factor and inductance trade off curves at 1 GHz, 2.4 GHz and 5 GHz

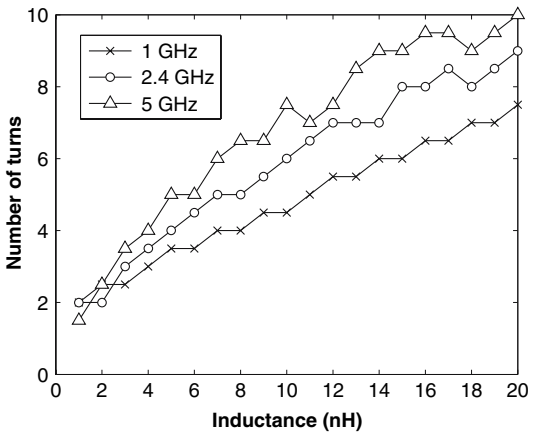

Fig. 13 Optimum number of turns versus inductance at 1 GHz, 2.4 GHz and 5 GHz

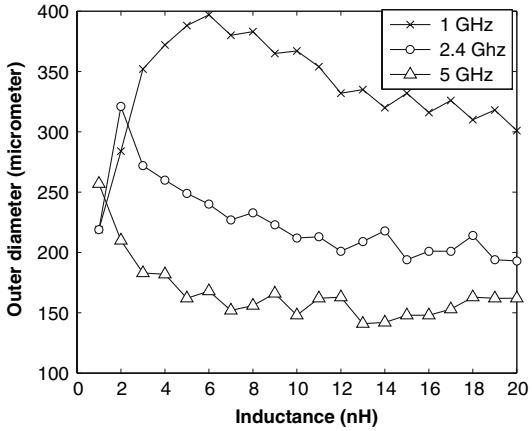

Fig. 14 Optimum outer diameter versus inductance at 1 GHz, 2.4 GHz and 5 GHz

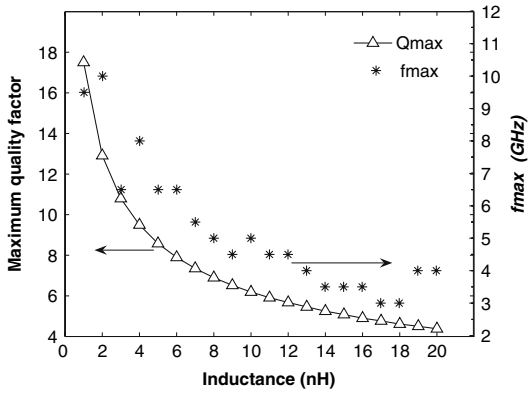

Fig. 15 Maximum quality factor and their corresponding peak frequency for inductance range 1 nH–20 nH

Table 4 being computed using a lumped element model, upon verification with a 3D electromagnetic simulator may result in slight error similar to that mentioned before for our design example of 6 nH at 2 GHz. However the error is within the manufacturing tolerance of spiral inductor realization [13].

4.1 Computation time

The optimization of 6 nH inductor discussed before is completed in 0.219 s of CPU time using the simple and accurate expression [20] for inductance calculation and 16.81 s of CPU time using Greenhouse method [16]. In enumeration method the time required for the optimization or the number of function evaluations will depend on the discretization of the design space (N, W and D_{out}). In our design example, we have chosen $11 \times 21 \times 98$ grid. The W and D_{out} was incremented by 1 μm, 4 μm, respectively and N was incremented by half turn each time. These step size

Table 4 Maximum quality factor and the corresponding optimum layout parameters

Inductance (nH)	Width (μm)	Turns	D_{out} (μm)	Q_{max}	f_{max} (GHz)
1	17	2	169	17.4	9.5
2	8	3	147	12.9	10.0
3	8	3.5	168	10.7	6.5
4	5	4.5	143	9.4	8.0
5	5	5	152	8.5	6.5
6	4	5.5	147	7.8	6.5
7	4	6	152	7.3	5.5
8	4	6.5	156	6.8	5.0
9	4	6.5	166	6.5	4.5
10	3	7.5	148	6.1	5.0
11	3	7	162	5.9	4.5
12	3	7.5	163	5.6	4.5
13	3	8	164	5.4	4.0
14	3	8.5	165	5.2	3.5
15	3	8.5	171	5.0	3.5
16	3	8.5	177	4.9	3.5
17	3	9	177	4.7	3.0
18	3	8.5	189	4.6	3.0
19	2	9.5	162	4.5	4.0
20	2	10	162	4.3	4.0

were chosen with assurance that optimum design was not missed out. The optimization method requires a total function evaluation of 5,393. Since the quality factor was calculated only at the combinations which results $L = 6$ nH the quality factor function evaluation is only 175. But an enumeration method without layout parameter bounding and with the same design constraints would require a total function evaluation of 37,044. This will again increase for an arbitrarily decided constraints and may require as large as million function evaluations [13]. Therefore with layout parameter bounding, a large proportion of the sample points that are redundant for a desired inductance value is pruned off and the number of function evaluations is reduced significantly.

In Table 3, a comparison of the computation time is also included. Geometric programming (GP) takes the minimum time of less than a second, among the numerical methods. The computation time of our proposed method is comparable to GP but less than other methods. Also, the global optimization of inductance range 1 nH–20 nH as discussed before, is completed in 6.40 s of CPU time. To compare the computation time with GP more closely, we have also implemented geometric programming algorithm [10]. For the same inductance range, with the same technological parameters, geometric programming performs the optimization in 7.36 s of CPU time. The global optimal trade off comparison at 2.4 GHz is shown in Fig. 16.

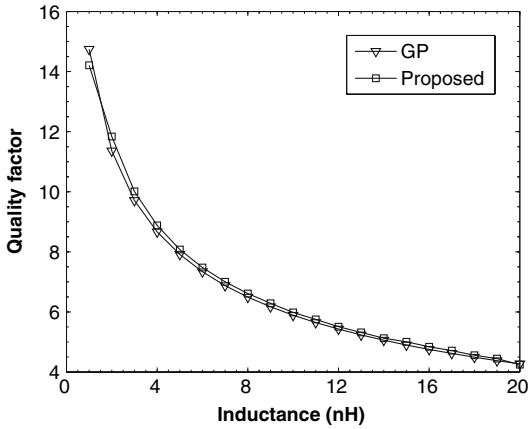

Fig. 16 Comparison of global optimal trade off curves for inductance range 1 nH–20 nH at 2.4 GHz (GP—geometric programming)

Moreover if a field solver, which requires an average simulation time of 5 min per frequency point, is used to get the same result it may take several days. Therefore, with layout parameter bounding, the computation time of an enumeration method is even less than or comparable to other numerical algorithms of [10, 12, 13].

5 Summary and conclusion

We have developed an efficient method of bounding the layout design parameters of on chip spiral inductor viz. number of turns (N), spiral track width (W), spiral track spacing (S), outer diameter (D_{out}) or inner diameter (D_{in}). The bounding algorithm results several curves for various width as a function of number of turns and the selection of upper and lower bounds of optimization variables was done graphically. With bounding curves the feasible region of optimization of a large inductance range that satisfies the same area specification was identified. An enumeration optimization algorithm was implemented based on layout parameter bounding. The number of function evaluations was significantly reduced and optimization took less than 1 s of CPU time. The results of optimization was also verified using a 3D electromagnetic simulator. Since the feasible region for any desired inductance value is determined apriori the optimization results in global solution and the method is very fast. Since bounding curves can be tailored to include all the desired range of inductance the method is more advantageous when multiple inductors of different values are to be optimized. Several important fundamental tradeoff of the design like quality factor and area, quality factor and inductance, quality factor and operating frequency, maximum quality factor and the peak frequency etc. for inductance values ranging from 1 nH–20 nH were explored in few seconds. With layout parameter bounding, enumeration method is proved to be as fast as other numerical algorithms. Enumeration method always results in a global optimum solution as compared to other numerical algorithms that may sometimes lead to non convergence and local optimum solutions. Hence with layout parameter bounding, optimum spiral inductors can be synthesized and analyzed in an easy and simple manner in few seconds.

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References

1. Bennett, H. S., Brederlow, R., Costa, J. C., Cottrell, P. E., Huang, W. M., Immorlica, A. A., Mueller, J. E., Racanelli, M., Shichijo, H., Weitzel, C. E., & Zhao B. (2005). Device and technology evolution for silicon-based RF integrated circuits. *IEEE Transactions on Electron Devices, 52*, 1235–1258.
2. Abidi, A. A. (2004). RF CMOS comes of age. *IEEE Journal of Solid-State Circuits, 39*, 549–561.
3. Burghartz, J. N. (2001). Status and trends of silicon RF technology. *Microelectronics Reliability, 41*, 13–19.
4. Long, J. R., & Copeland, M. A. (1997). The modeling, characterization, and design of monolithic inductors for silicon RF IC's. *IEEE Journal of Solid-State Circuits, 32*, 357–369.
5. Koutsoyannopoulos, Y. K., & Papananos, Y. (2000). Systematic analysis and modeling of integrated inductors and transformers in RF IC design. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 47*, 699–713.
6. Andersen, R. B., Jorgensen, T., Laursen, S., & Kolding, T. E. (2002). EM-simulation of planar inductor performance for epitaxial silicon processes. *Analog Integrated Circuits and Signal Processing, 30*, 51–58.
7. Haobijam, G., & Paily, R. (2006). Systematic analysis, design and optimization of on chip spiral inductor for silicon based RFIC's. In *IEEE INDICON 2006 Conference*, India.
8. Niknejad, A. M., & Meyer, R. G. (1998). Analysis, design, and optimization of spiral inductors and transformers for Si RF IC's. *IEEE Journal of Solid-State Circuits, 33*, 1470–1481.
9. Post, J. E. (2000). Optimizing the design of spiral inductors on silicon. *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, 47*, 15–17.
10. Hershenson, M. M., Mohan, S. S., Boyd, S. P., & Lee, T. H. (1999). Optimization of inductor circuits via geometric programming. In *Proc. of the IEEE ACM Design Automation Conference*, pp. 994–998.
11. Kim, J., Lee, J., Vandenberghe, L., & Yang, C.-K. (2004). Techniques for improving the accuracy of geometric-programming based analog circuit design optimization. In *Proc. of the Int. Conf. Comput. Aided Des.*, pp. 863–870.

12. Zhan, Y., & Sapatnekar, S. S. (2004). Optimization of integrated spiral inductors using sequential quadratic programming. In *Proc. of the IEEE Design, Automation and Test in Europe Conf. and Exhibition*.
13. Nieuwoudt, A., & Massoud, Y. (2006). Variability-aware multilevel integrated spiral inductor synthesis. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 25*, 2613–2625.
14. Bhaduri, A., Vijay, V., Agarwal, A., Vemuri, R., Mukherjee, B., Wang, P., & Pacelli, A. (2004). Parasitic-aware synthesis of RF LNA circuits considering quasi-static extraction of inductors and Interconnects. In *Proc. of the 47th Midwest Symp. Circuits and Syst*., pp. 477–480.
15. Mukherjee, S., Mutnury, B., Dalmia, S., & Swaminathan, M. (2005). Layoutlevel synthesis of RF inductors and filters in LCP substrates for Wi-Fi applications. *IEEE Transactions on Microwave Theory and Techniques, 53*, 2196–2210.
16. Greenhouse, H. M. (1974). Design of planar rectangular microelectronic inductors. *IEEE Transactions on Parts, Hybrids and Packaging, Php-10*, 101–108.
17. Sia, C. B., Hong, B. H., Chan, K. W., Yeo, K. S., Ma, J. G., & Do, M. A. (2005). Physical layout design optimization of integrated spiral inductors for silicon-based RFIC. *IEEE Transaction Electron Devices, 52*, 2559–2567.
18. Yue, C. P., & Wong, S. S. (2000). Physical modeling of spiral inductors on silicon. *IEEE Transaction Electron Devices, 47*, 560–568.
19. Farina, M., Rozzi, T. (2001) A 3-D integral equation-based approach to the analysis of real-life MMICs-application to microelectromechanical systems. *IEEE Transaction Microwave Theory Techinques, 49*, 2235–2240.
20. Mohan, S., Hershenson, M., Boyd, S., & Lee, T. (1999). Simple accurate expressions for planar spiral inductances. *IEEE Journal of Solid-State Circuits, 34*, 1419–1424.

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