General MEMS Process Physics Simulation and its Applications

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ABSTRACT

Commercial CAD tools for MEMS have significantly contributed to the growth that the MEMS industry has experienced over the past two years by reducing development cycles and enabling the more rapid release of mature MEMS products. Unfortunately, the CAD for MEMS industry has focused primarily on device performance (for example, mechanical response due to electrostatic loading), with a concentration on testing and optimizing the performance in a workstation environment. Device manufacturability issues have been neglected and considered secondary design criteria.

Understanding device fabrication is essential in determining if an optimized device design can be realized in a cost-effective manner using current microfabrication equipment. Research has been undertaken to identify key process steps in MEMS fabrication that can play a role in device behavior. The release of commercial anisotropic etch simulation code has proven the utility of process simulation[1].

IntelliSense has developed a general MEMS process physics simulation capability that addresses key process steps in both surface and bulk MEMS fabrication. Process simulation modules developed include: thin film deposition; wet and dry etching; bonding; micro-assembly; doping; electroplating; and liftoff. These processes are simulated both physically and semi-empirically. As a result, the geometric shape, incorporating both the material properties and the process induced effects, is efficiently generated and transitioned to a multi-physics analysis module or system level analysis gateway.

Accounting for process-induced effects when simulating the performance of device designs allows for greater accuracy, which in turn helps reduce product development times beyond the capabilities of current CAD tools for MEMS.

Keywords: MEMS, process simulation, process physics, CAD, fabrication

1 INTRODUCTION

Until now, CAD tools for MEMS have focused on geometric representation from the process in order to analyze device behavior. The drawback of this simulation method is that process induced effects may vary the geometry of the structure significantly. For example, the boron diffusion as an etch stop layer for bulk silicon processing may overstress the structure, or a silicon glass bonding process may breakdown the oxide film.

A comprehensive process simulation module must incorporate deposition, etching, bonding, doping, electroplating, liftoff, and other process steps common in MEMS design. Other process induced effects, such as micro-assembly, must be addressed to generate accurate geometric models for the complete range of MEMS devices. These key processes must be simulated physically so that such side effects are accounted for in the design.

IntelliSense has developed a general MEMS process physics simulator, in which separate modules address the different process related concerns and then integrate seamlessly to produce the final device design. A MEMS design, generated from true process physics simulation, will results in a readily manufacturable and high yield device design.

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2 PROCESS SIMULATOR ARCHITECTURE

Figure 1 shows the global dataflow inside of the MEMS process simulator. First, the process physics simulator receives data from the process table (including the process parameters and mask layouts). Next, the three dimensional geometry is automatically generated and the physical processes are checked for each key MEMS process. The global process is then checked to see if the structure is overstressed, the insulator layer is breaking down, the KOH wet etching corner compensation features are not properly designed, etc. Note that this is not a design rule check for layout, but a physics related process design check. A final check is performed on the geometry of the structure for micro-assembled devices.

Once all of the physics and geometric checks are completed, the device is ready for behavioral analysis. Also, with this procedure, modifications made to the design based on the device performance analyses will be checked for process and geometric accuracy.

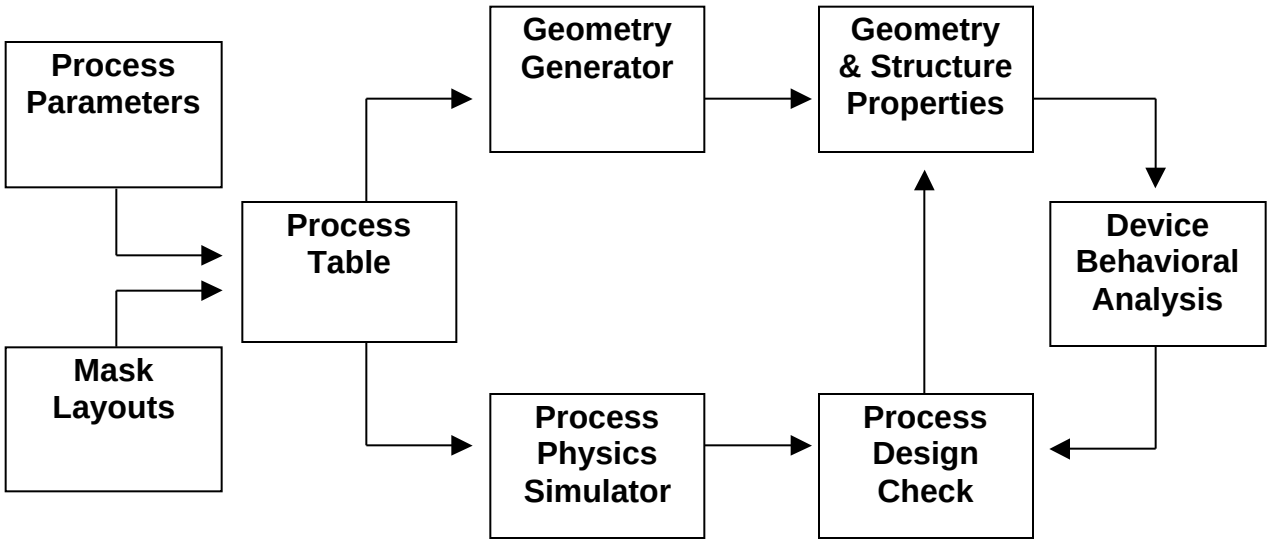

Figure 1 Process simulation architecture

3 PROCESS SIMULATION

3.1 Deposition

Accurate modeling of deposition steps requires the accurate modeling of the deposited material itself. Unlike bulk material properties, the thin-films of material used in MEMS manufacturing have properties which can be difficult to characterize and for which little data is readily available. IntelliSuite™ includes MEMaterial®, an extensive thin-film material database, to give engineers ready access to material properties. The incorporation of this more accurate data is the first step towards a more accurate device model.

3.2 Oxidation

Oxidation is one of the primary layering operations in silicon technology. Silicon dioxide layers are used for passivation of silicon surfaces, masks for diffusion and ion implantation, dielectric films, and interface layers between the substrate and other materials such as in chemical or biosensors[2].

The oxidation process in IntelliSuite™ is simulated using combined analytical and empirical models that account for the influences on the oxidation rate such as wafer orientation, wafer dopant distribution type, and the oxide time and temperature. The result is an accurate geometry with correct thicknesses and material properties for both the original silicon and the simulated oxide layer. The corresponding protective and dielectric effects are then accounted for at later stages of the design.

3.3 Diffusion

N-P or P-N junctions resulting from diffusion behave differently from the original wafer. The depth of this junction and the associated properties can now be modeled in IntelliSuite™. An example of the use of such a junction in MEMS fabrication is an etch stop for bulk silicon etching. The etch stop created a protected region around which etchant is free to flow to create suspended elements in the device (see Section 3.6).

3.4 Annealing

Annealing is a high-temperature processing step designed to minimize stress in the crystal structure of the wafer. After ion implantation, the dopant atoms cause a disruption of the wafer crystal structure. Annealing the wafer, heat treating, at high temperature can repair this damage. Another annealing step typically occurs after conducting strips of metal, to carry the electrical current between the device and the circuit, are formed on the wafer.

Annealing affects the residual stresses, which can have a substantial impact on the functionality of the device. IntelliSuite™ therefore corrects the properties in each affected layer during the process design check phase.

3.5 Wafer Bonding

Wafer bonding processes are physically simulated within IntelliSuite™ to determine the effect of the bonding process on previously deposited material layers. IntelliSuite™ analyzes the bonding process electric field distribution versus bonding time and temperature. Modeling the physical process within the virtual environment enables engineers to address potential problems, such as breakdown in an oxide layer, prior to fabrication. This results in a device design which is optimized for manufacturing with high yield rates.

3.6 Anisotropic Etching

A final aspect of IntelliSuite's process physics simulation capabilities is AnisE®[1], the anisotropic etch simulator. AnisE® enables engineers to accurately model the final three-dimensional geometry of bulk silicon etched structures. These can be difficult to estimate if elements such as multiple etch stops and corner compensation have to be included.

The following figures show three examples of AnisE® results as compared to actual SEM images. In each case an etch stop has been applied to create the geometry. Figure 2 shows two crossed beams. The edge characteristics are apparent as is the lack of release in the center. Figures 3 and 4 show cantilever structures. AnisE® has accurately predicted the difference in undercutting that occurs because of the angle of the beams to the wafer.

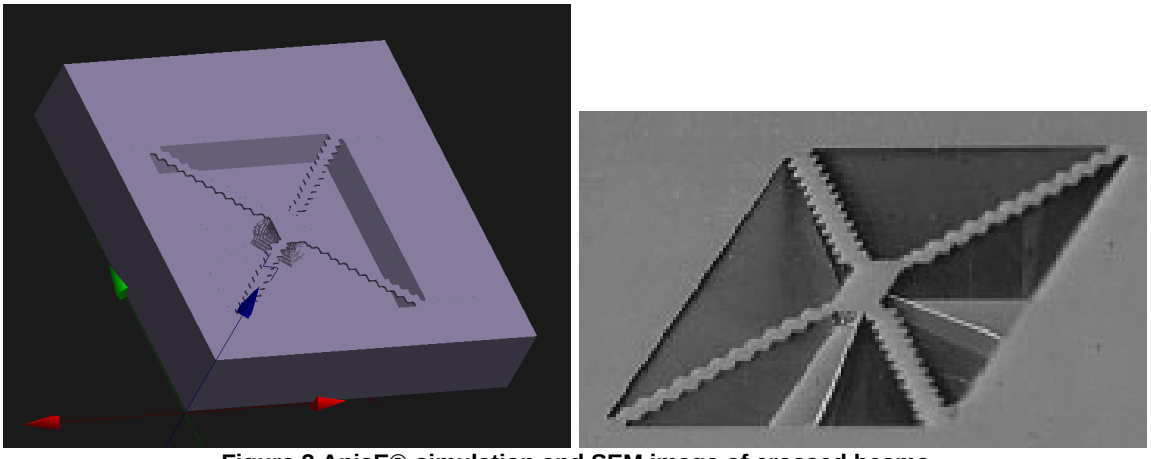

Figure 2 AnisE® simulation and SEM image of crossed beams

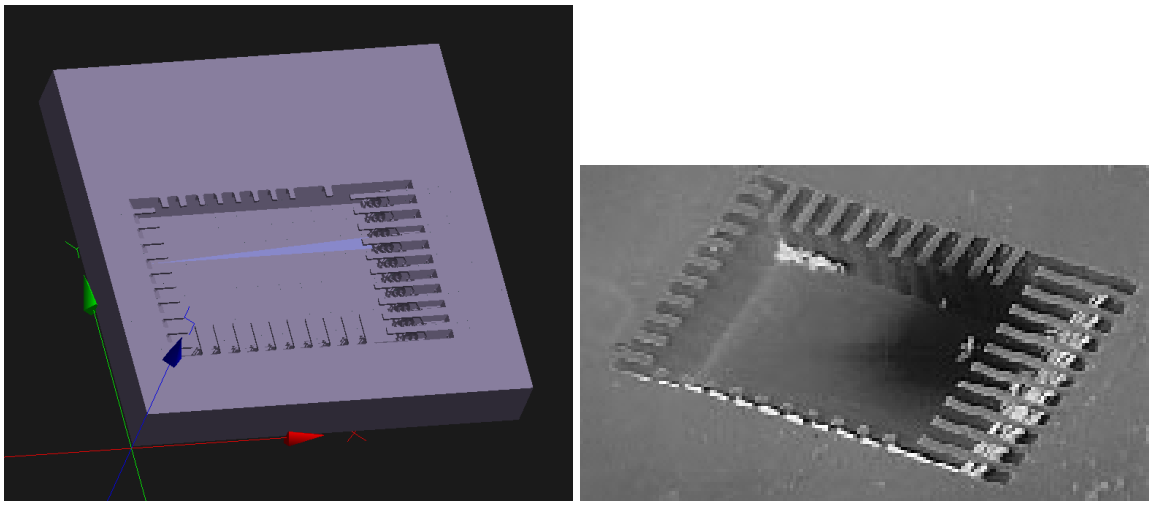

Figure 3 AnisE® simulation and SEM image of right-angle cantilever beams

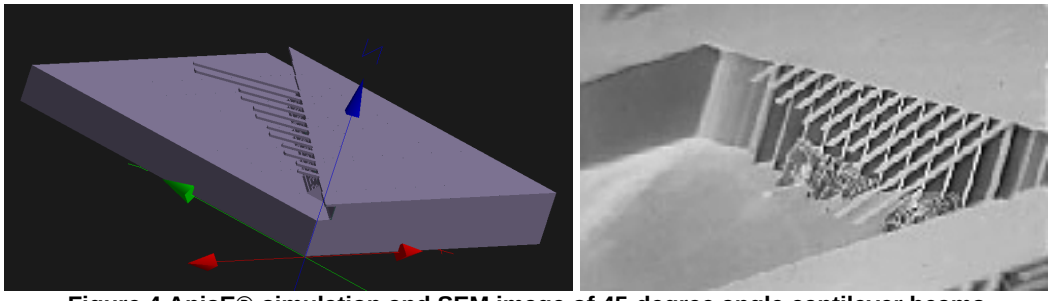

Figure 4 AnisE® simulation and SEM image of 45-degree angle cantilever beams

AnisE® also predicts corner compensation, a feature which is often neglected or miscalculated during the design process. Figure 5 shows a mask and the resulting AnisE® simulation (The mask layout appears above the final structure.). On both elements, the lower right has not been protected and hence has been rounded during the etch. On the element in the upper left, narrow corner compensation features have increased the degree of protection (proceeding counter clockwise from the upper right) but have not completely protected the corner. In contrast, the widening of these features does finally result in a fully protected corner. Note that the length of the corner compensation feature is the same for the corresponding corners on both elements.

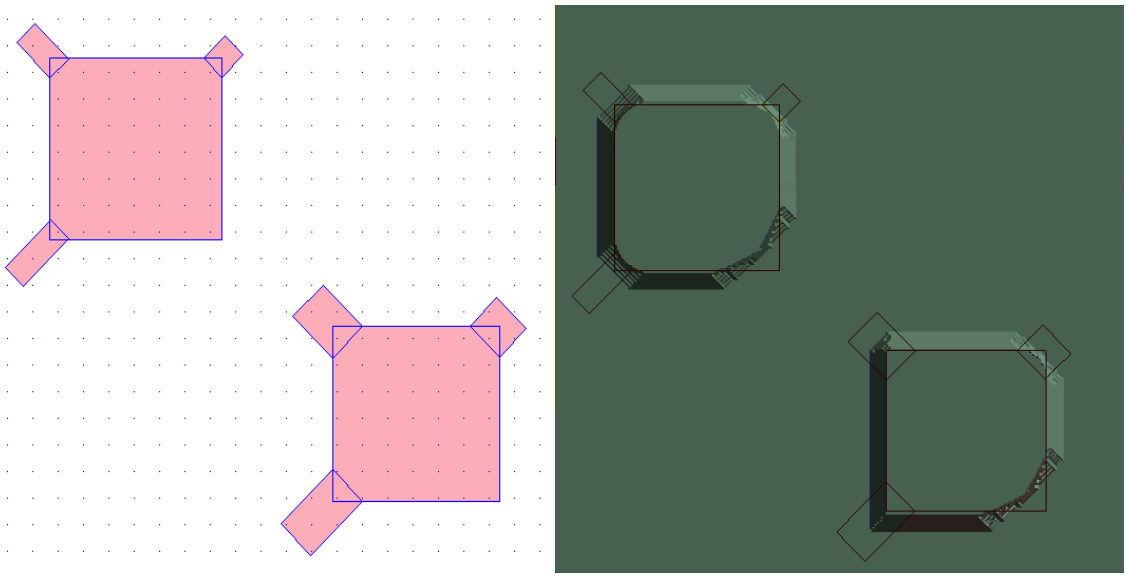

Figure 5 Corner compensation mask and the corresponding AnisE® simulation results

4 CONCLUSION

Through true physics process simulation, IntelliSuite™ is now able to accurately model both the three-dimensional geometry and material properties of a MEMS structure directly from the process. This enables engineers to more accurately model the device behavior, especially as relates to process induced effects such as induced stresses, bulk silicon geometries, and oxide breakdown.

Accounting for process induced effects during simulation, enables the creation of a more accurate model and thereby reduces product development time. By using a unique process simulation architecture which analyses each of the processes in turn as well as in relation to other processes, IntelliSuite™ enables engineers to design devices optimized for high yield manufacturing.

REFERENCES

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