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Coupled Electromechanical and Full Wave Electromagnetic Analysis of Micromachined Electromechanically Tunable Capacitors

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Abstract

This research work presents the simulation-based electromechanical and electromagnetic analyses of two-plate and three-plate CMOS voltage-controlled oscillators (VCOs). These oscillators, described in [1,2,3], use electromechanically tunable capacitors fabricated using the MUMPs process [4] and integrated inductors. Numerical models for each capacitor design were constructed using appropriate dimensions and material properties. The effects of process-induced stresses and electrostatic fringing fields were incorporated in the design analyses of the capacitors [5]. Coupled electromechanical analyses were performed to measure the behavior of the tunable capacitors as a function of the applied voltages. The two-plate capacitor has a nominal capacitance of 2.05 pF, is tunable to 3.08 pF, and has a Q-factor of 20 at 1 GHz and 11.6 at 2 GHz. The three-plate capacitor has a nominal capacitance of 4.0 pF, is tunable to 7.4 pF, and has a Q-factor of 15.4 at 1 GHz and 7.1 at 2 GHz. The electromagnetic analyses were performed using the Generalized Transverse Resonance-Diffraction (GTRD) method, a 3D integral equation approach well suited for quasi-planar structures involving thick conductors and dielectric discontinuities [5,6]. Structures of this type usually prove to be challenging for standard 3D techniques (e.g. Finite Elements, Finite Differences, etc.) owing to their critical aspect ratio, while being ill-suited for the so-called 2.5 techniques, in which conductor thickness and dielectric discontinuities are hardly accounted for. The combination of electromechanical and electromagnetic simulations presented in this paper allows for complete analysis and optimization of RF MEMS devices to be performed at the simulation stage.

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Introduction:

Electrically tunable capacitors have a wide range of applications, ranging from tunable antennas, to reconfigurable filters and low-noise voltage-controlled oscillators (VCOs). Any of those applications require high quality tunable resonators in order to comply with the system requirements of currently used communication systems, such as GSM. At the same time, they should meet the integration specifications needed to develop Systems on Chip (SoC). However, high-Q resonators are generally difficult to integrate onto the same chip as the other parts of the system. Use of MEMS-based variable capacitors has been shown to provide high-Q factors and wide tuning range capabilities. The MEMS-based variable capacitors can result in low phase-noise VCOs and have the capability to handle large voltage swings. Dec and Suyama [1] have demonstrated MEMS based two-and-three plate tunable capacitors and an integrated inductor in the 1-2 GHz band (see figure 1). These devices were fabricated using the MUMPS process [4] and show a Q-factor of 20 and 15.4 (at 1 GHz) for two and three-plate configuration respectively.

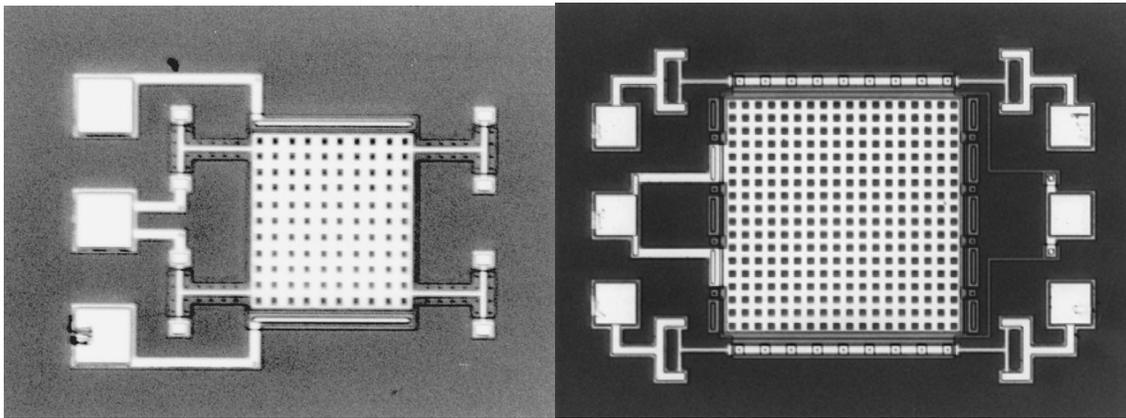


Figure 1: Micrograph of two and three plate tunable capacitor [1]

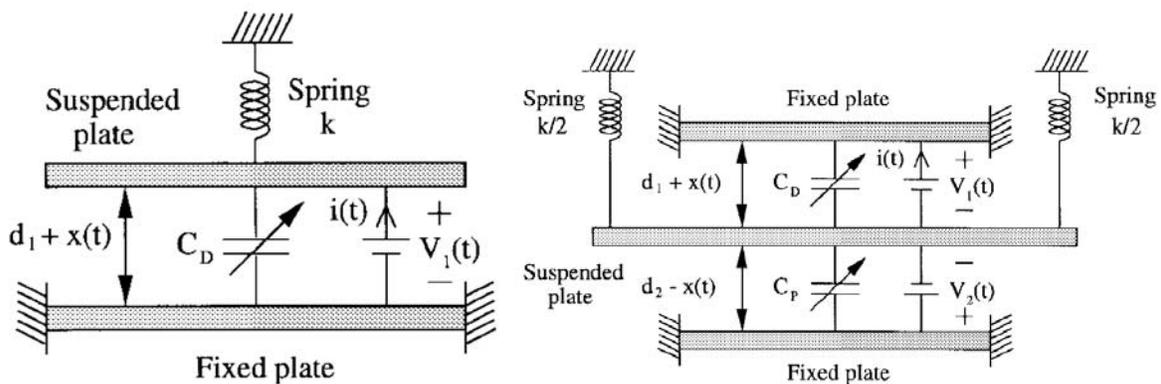


Figure 2: Functional representation of two and three plate tunable parallel-plate capacitors [1]

Figure 2 shows functional models of two and three plate electro-mechanically tunable capacitors. In the case of two-plate capacitor, the top plate of the capacitor is suspended by a spring with stiffness “ k ”, while the bottom plate of the capacitor is fixed. When a voltage bias $V_1(t)$ is applied across the parallel plate, the suspended plate starts to move

towards the fixed plate due to electrostatic attraction. The suspended plate can move upto a distance of one-third of initial gap [$d_1 + x(t)$] before it completely snaps onto the fixed plate as the mechanical restoring force can no longer overcome the electrostatic force. The maximum capacitance that such a tunable capacitor can be tuned to is $3/2 C_D$, and the maximum theoretical tuning range is 1.5:1. For a three plate tunable capacitor, the top and bottom plate are fixed, while the plate in the center can toggle between the two fixed plates when voltage bias $V_1(t)$ and/or $V_2(t)$ are applied. The movable middle plate is supported by two springs with a stiffness of $k/2$ each. The maximum capacitance is still $3/2 C_D$, but the minimum capacitance is now $3/4 C_D$. Thus theoretical tuning range for the three-plate capacitor is 2:1.

The research work being reported here introduces an accurate electromagnetic and electromechanical analysis of the abovementioned tunable capacitors. For the electromechanical analysis, the effects of process-induced stresses and electrostatic fringing fields are incorporated in the analyses of the capacitor [8]. Coupled electromechanical analyses are performed to measure the behavior of the tunable capacitors as a function of the applied voltages. The electromagnetic analysis was carried out by using GTRD [6], an integral equation approach which accounts for the finite thicknesses of conductors and dielectric discontinuities. To minimize the computational expense, the structure was divided into two parts, the pads and the capacitor, taking advantage of the Short-Open Calibration (SOC) technique introduced in [7]. Results are shown to be in good agreement with experimental values.

Theory:

Coupled electromechanical analysis is explained in detail in [5,8] and other references, and is well understood in the field of MEMS design and analysis. The fully three-dimensional analysis iterates between a mechanical finite element method (FEM) solution and an electrostatic boundary element method (BEM) solution. The final solution represents the structural orientation at which forces due to the electrostatic charge buildup (as well as any other applied loads) are exactly balanced by the mechanical restoring force of the structure. Non-linear FEM allows for process-induced effects such as residual stresses to be accounted for in the numerical model. The BEM accounts for the effects of electrostatic fringing fields, as well as the presence of multiple and varied dielectric insulators. Independent refining of the FEM and BEM models has proven to be an effective method for reducing overall model complexity without sacrificing numerical accuracy [8].

The GTRD based electromagnetic analysis approach has been introduced in [6]. The primary step is the calculation of the 3D Green's function of a multilayer dielectric stack. For this case, the whole structure is assumed to be enclosed in a box, to simplify the excitation of the structure and to gain the well-known high accuracy that a modal description allows. As an additional expedient, the Green's function is calculated in the spectral domain so as to avoid kernel singularity issues. Hence the first step is common to other spectral-domain method-of-moment (MoM) approaches. However, it has to be stressed that in this case the 3D Green's function relates volume current sources to the

electric field in the boxed stack. The ability to deal with volume currents enables the full 3D analysis of the structure, in contrast to the common “2.5 algorithms”. In addition, Ohm’s law must be satisfied by the current sources within the conductors. Other laws may be used to set up the final integral equation, and general displacement currents are used to define dielectric discontinuities [6]. Standard delta-gap excitation is used to extract the network parameters, while an evolution of SOC introduced in [7] allows the removal of the discontinuity related to the port definition. The main feature of GTRD is the ability to perform a full 3D analysis while being well suited for quasi-planar structures having complex substrates. The direction of the dielectric stratification (e.g., vertical) does not impose any constraints on aspect ratio, a common limiting factor in space-discretization techniques.

The inherent accuracy of the SOC technique allows the structure to be split into simpler subsections, so even the limits related to the horizontal aspect ratio are overcome. In this case a separate analysis of the pads has been performed. The pads are known to have a measurable impact on device performance. This is quite obvious, considering that a standard pad from a MUMPs process results in 1.5 pF capacitance, while the designed tunable capacitor has a nominal value of 0.6 pF. In [1] a low-capacitance pad was introduced, showing just 0.25 pF parasitic capacitance, and this pad is addressed in the following sections. Once separate simulations for the pads and the tunable capacitor are available, the overall performances are recovered by combining the simulations at the circuit level.

Electromechanical Analysis:

Accurate and efficient coupled electromechanical analysis relies on the geometry and material properties of the device, a refined finite element mechanical mesh in areas of high stress and/or deformation, and a refined boundary element electrostatic mesh in areas of high electrostatic charge density buildup. The effects of the residual stress in the polysilicon structural layers due to the deposition process cannot be ignored. Other assumptions, such as rigid-body motion of the moving plate, are inaccurate and will affect the performance of the device. Electromechanical simulations were used to measure the tunable range of the capacitor, as well as various mechanical effects, including pull-in voltage and resonant frequency tuning.

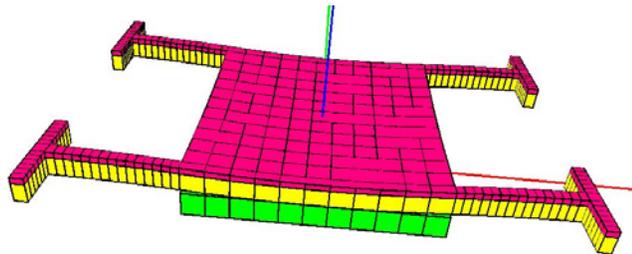


Figure 3: Deformation due to intrinsic stresses (magnified for illustration purposes)

Process induced effects cannot be neglected in the design or analysis of a MEMS device. As the capacitors in [1] were fabricated using the MUMPs process, it is likely that there is a residual stress present in the polysilicon layers of the capacitor plates. From the PolyMUMPs run data [4], the residual stress in both the Poly1 and Poly 2 layers varies between 0 and 20 MPa compressive, with a typical value of approximately 10 MPa compressive. This residual stress will tend to cause the membrane to bow, as shown in Figure 3. Further, this compressive stress may reduce the effective stiffness of the

membrane, causing the device to pull-in at a lower voltage. The effect of residual stress on the unbiased capacitance (due to change in airgap) is shown in Figure 4.

The design parameters used in the previously reported research [1] assume that the moving plate in each capacitor design will move as a rigid body. That is, the beams will bend, but the capacitor plates will move without deforming. Due to the high width-to-thickness ratio of these plates, this assumption is not valid. Figure 5 shows the first mode of vibration for both the two-plate and three-plate capacitor designs. The plates can clearly be seen to be deforming along with the beams. As a result, the effective stiffness of the systems (and the frequencies of oscillation) will decrease, as will the voltages required to cause pull-in. Fully coupled electromechanical analyses were performed on both the two-plate and three-plate capacitor designs without the aforementioned rigid-body assumption.

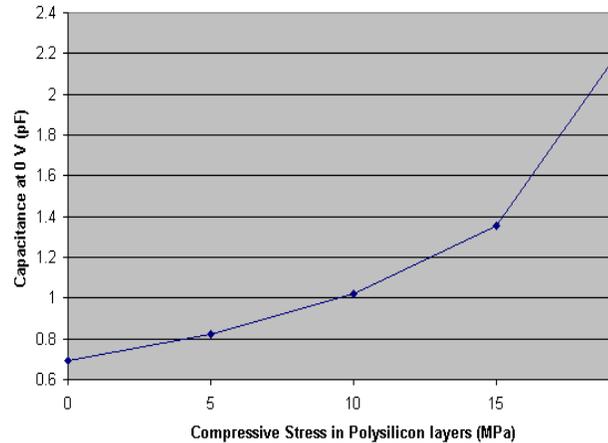


Figure 4: Capacitance as a function of intrinsic stress

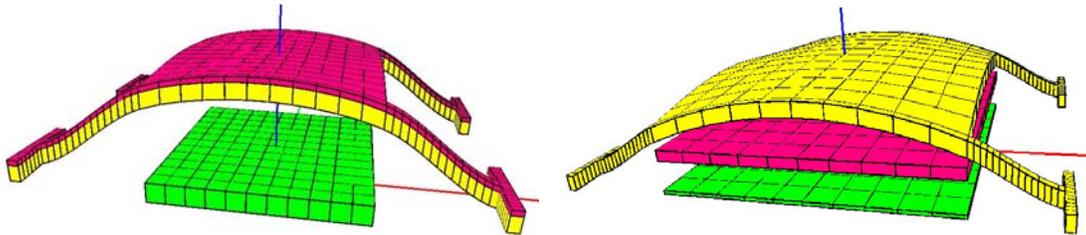


Figure 5: First vibrational modes for two- and three-plate VCOs (magnified for illustration)

Two-plate capacitor

The first simulation performed was a natural frequency analysis. The natural frequency was 23.1 kHz when neglecting the residual stresses, lower than the value of 39 kHz predicted in the research [1]. Incorporating a 10 MPa compressive stress in the polysilicon and a 20 MPa tensile stress in the gold increased the natural frequency slightly to 23.6 kHz. In addition, this frequency is dependent on the voltage load being applied to the capacitor. The second simulation performed was a pull-in analysis. The voltage differential between the plates was increased until the moving plate contacted the ground plane. A more refined analysis was then performed near the pull-in voltage to accurately capture the relationship between the applied voltage and the resulting capacitance up to the point of pull-in. As observed experimentally, the tuning ratio was approximately 1.5:1. The results for the natural frequency of vibration and the capacitance as functions of voltage are shown in Figure 6. Pull-in occurred at approximately 2 V.

Three-plate capacitor

The three-plate VCO was also simulated. Again, the first simulation performed was a natural frequency analysis. As the moving plate had an even higher width-to-thickness ratio in this case, the effects of relaxing the rigid-body assumption were even more significant. The natural frequency was 20.3 kHz when neglecting the residual stress, much lower than the predicted value [1] of 65.8 kHz. Incorporating a 10 MPa compressive stress in the polysilicon further reduced the natural frequency to 19.1 kHz. Again, this frequency is dependent on the voltage load(s) applied. Pull-in analyses were also performed to determine the pull-in voltage as well as the capacitance values as a function of the applied voltages. As observed experimentally, the three-plate capacitor has a higher tuning ratio. The analyses showed a tuning ratio of 2.4:1, however the minimum capacitance value was obtained at the threshold of instability. Figure 7 shows the natural frequency of vibration and the capacitance as functions of voltage. Pull-in occurred when a 1.1 V load was applied to the top plate or a 2.81 V load was applied to the bottom plate.

Electromagnetic Analysis:

Generalized Transverse Resonance-Diffraction (GTRD) technique relies on availability of the Green's function of a boxed dielectric stack, and the final integral equation is obtained by imposing Ohm's law in conductor regions. Standard delta-gap excitations are used in order to define ports, and the Method of Moments (MoM) is finally used to solve the integral equation that, in the most general (passive) case, is

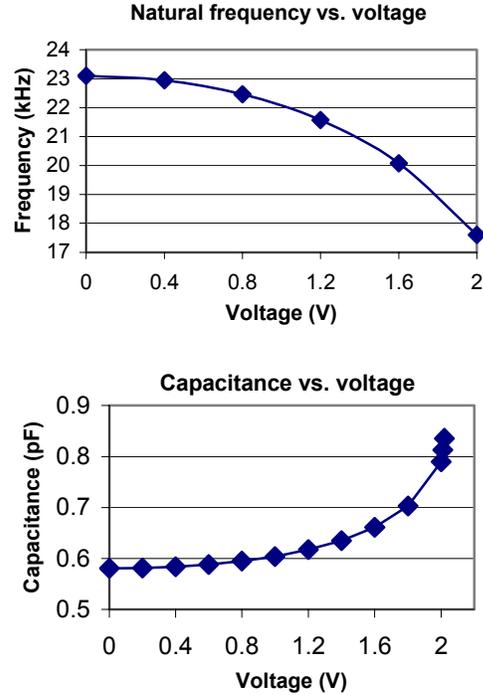


Figure 6: Two-plate VCO behavior as a function of applied voltage

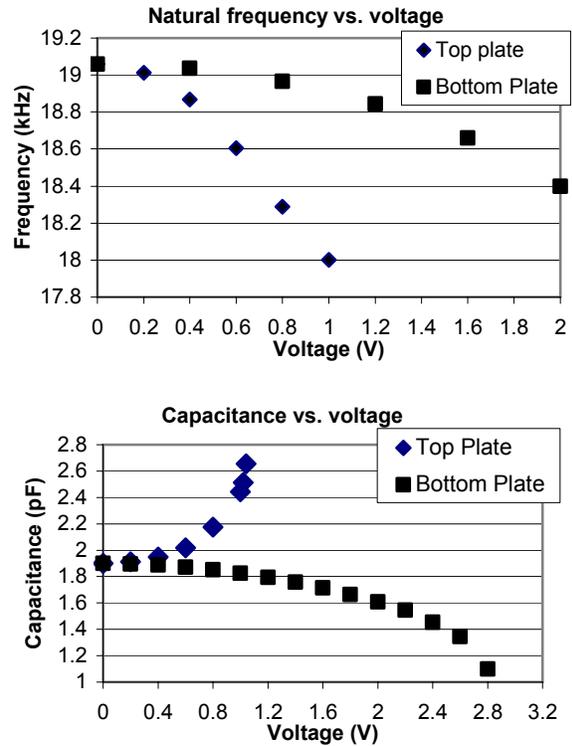


Figure 7: Three-plate VCO behavior as a function of applied voltages

$$\iiint_V d\mathbf{r}' \left[\mathbf{Z}(\mathbf{r}, \mathbf{r}') + \frac{1}{j\omega\epsilon_0(\tilde{\epsilon}(\mathbf{r}) - \tilde{\epsilon}'(\mathbf{r}))} \mathbf{I}(\mathbf{r}, \mathbf{r}') \right] \cdot \mathbf{J}(\mathbf{r}') = \delta(v - v_0) \text{rect}(p) \mathbf{u} \quad (1)$$

In the above equation \mathbf{Z} is 3D Dyadic Green's Function of the dielectric stack, $\tilde{\epsilon}$ is the complex dielectric permittivity defining either a lossy conductor or a dielectric brick, $\tilde{\epsilon}'$ the permittivity of the embedding substrate, v is any of the Cartesian co-ordinates, \mathbf{u} is unitary vector orthogonal to v and $\text{rect}(p)$ is an unitary function across the conductor section defining port p . The integral equation is solved by expanding currents by a set of piece-wise sinusoidal functions along their propagation direction and piece-wise constant along the remaining ones; piece-wise functions are defined over a sub-domain grid (mesh).

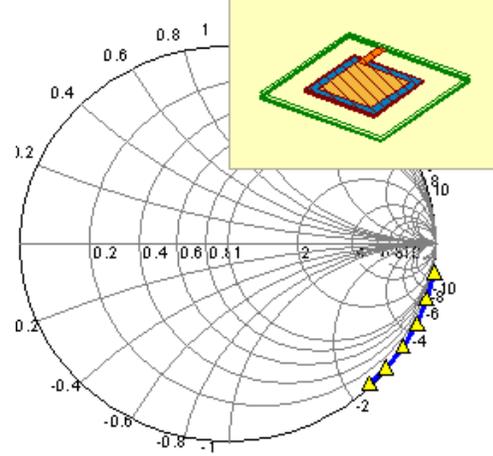


Figure 8: Smith's chart of S11 for the two-plate capacitor (pad)

The impulsive impressed field also behaves as a discontinuity for the electromagnetic field, inducing a local reactive storing of energy. Such an effect has to be calibrated out, mostly as done by the calibration procedure in a network analyzer. Hence some additional analysis of "standard" structures has to be performed. In our work a new short-open calibration algorithm has been used: this was developed as generalization of the work in [7] and it is described in detail in [9]. It takes advantage of the knowledge of the current distribution as output of the MoM in order to reduce by one half the number of standards to be analyzed for the full-calibration. The reduction of the number of independent analyses also results in an intrinsically larger numerical stability.

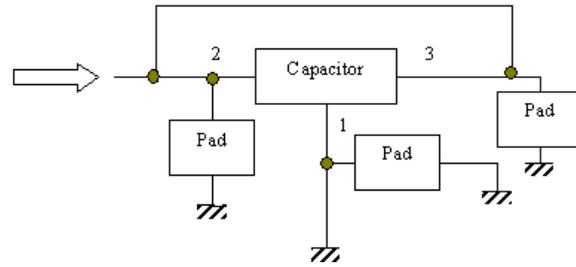


Figure 9: Topology used to evaluate the electromagnetic performance of the capacitor

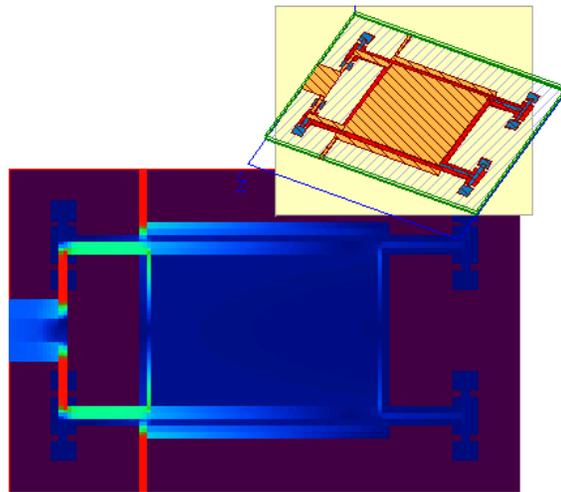


Figure 10: Volume current density distribution (all layers)

By using the calibration algorithm, the tunable capacitor and its pads are

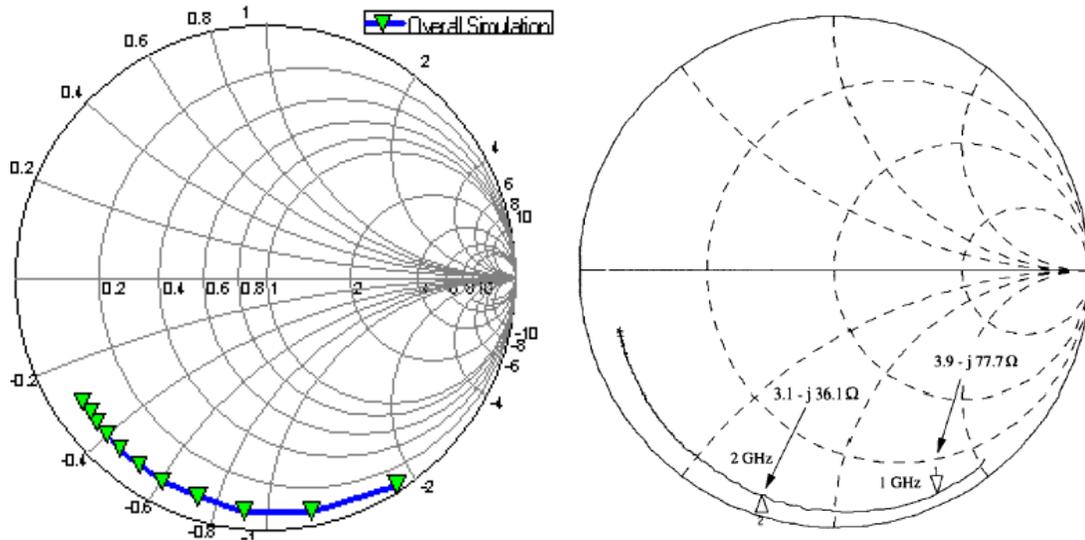


Figure 11: Simulated (left) and reported [1] (right) S-parameters for 1-6 GHz

modeled separately in order to minimize the computational expense. The overall frequency response is then evaluated by combining the results at the circuit level. The pads are of primary importance, owing to their parasitic capacitance, often of the same order of magnitude as--or even larger than--the tunable capacitor itself. In [1] a new pad design was introduced: while a standard pad in the MUMPs process has a 1.5 pF parasitic capacitance, the proposed topology was designed to have only 0.25 pF. It is an 86x86 μm square pad, consisting of a 1.5 μm polysilicon layer (sheet resistance 20 Ω/sq) and a 0.5 μm gold layer over a 2.25 μm oxide layer. A rectangular ring beneath the pad (anchor) encloses the oxide region. The whole structure is above a 0.6 μm silicon nitride layer ($\epsilon_r=7.6$) and a very conductive silicon substrate, behaving as a ground. The calculated reflection coefficient about the pad is shown in Figure 8 over a Smith's chart, in the frequency range 1-6 GHz; simple calculation shows that the structure behaves like a 0.226 pF capacitor and that the critical parameter affecting such a result is the conductive ring.

The device was simulated according to Figure 9. The two plate tunable capacitor and the total (volume) current density distribution calculated at 1 GHz are shown in Figure 10. Six layers were used in order to describe the whole capacitor: layer 1 is the gold layer, layer 2 is polysilicon, layer 3 is the 0.75 μm spacing (no actuation voltage applied), layer 4 is polysilicon, layer 5 is air spacing, and layer 6 is silicon nitride. The whole

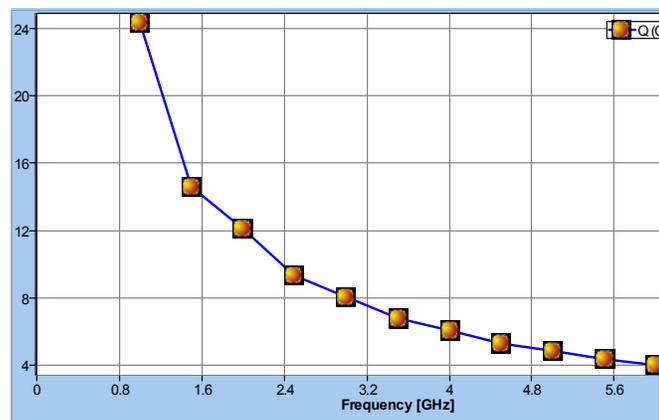


Figure 12: Simulated "Q" quality factor

structure is placed over a conductive substrate. The design value is 0.6 pF. Figure 11 compares simulated and measured [1] S parameters, highlighting a very good agreement in both modulus and phase. The agreement in phase is, in many cases, also an indicator of the quality of the de-embedding procedure, as any extra-electrical length would contribute to a larger phase difference. The quality factor in this work is calculated according to the definition:

$$Q = \frac{\Delta}{|\text{Im}(Y_{11}) / \text{Re}(Y_{11})|} \quad (2)$$

The calculated value for this parameter is reported Figure 12 as function of the frequency. At 2 GHz it is 12.2, in excellent agreement with the measured value, reported in [1] to range around 11.6. This agreement witnesses the ability of the electromagnetic model to account for ohmic losses.

Conclusions:

The electromechanical and electromagnetic behavior of two- and three-plate tunable capacitors has been simulated. The devices, which were fabricated using the MUMPs process, were simulated using the IntelliSuite™ software. The results of the analyses agree very well with the experimental data. Assumptions were lifted during the electromechanical analysis, allowing for the inclusion of residual stress and non-rigid body motion. The electromagnetic analysis predicted the Q-factors within 5%. Slight differences in the pull-in voltages are probably due to the parasitic capacitance of the substrate, which was neglected in the analyses. Also, thin film material properties and process variation in layer thicknesses could have caused the experimental results to differ from the expected and simulated results. For future designs, the use of these simulations can provide valuable information that can be used to optimize the performance of the MEMS device. Non-linear factors, such as the effect of residual stress, non rigid-body motion of the capacitor plates, conductor thickness, and dielectric discontinuities can be investigated quickly and efficiently without the cost of a fabrication run.

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