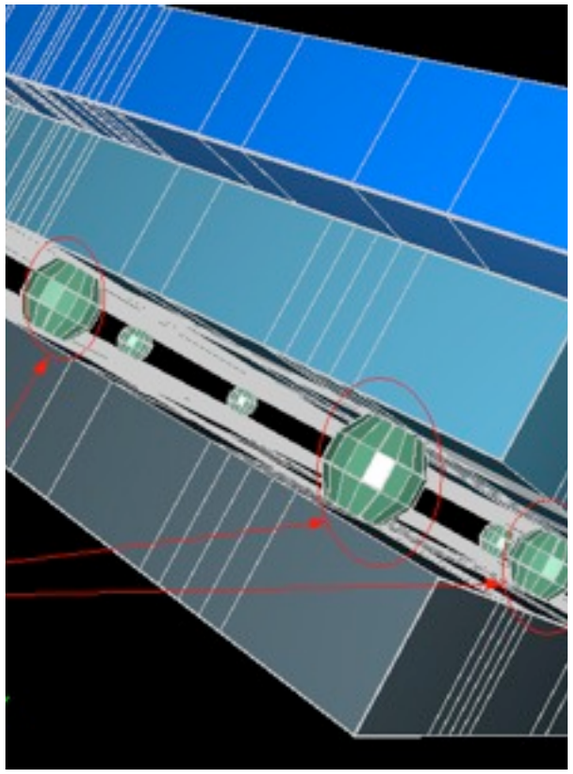
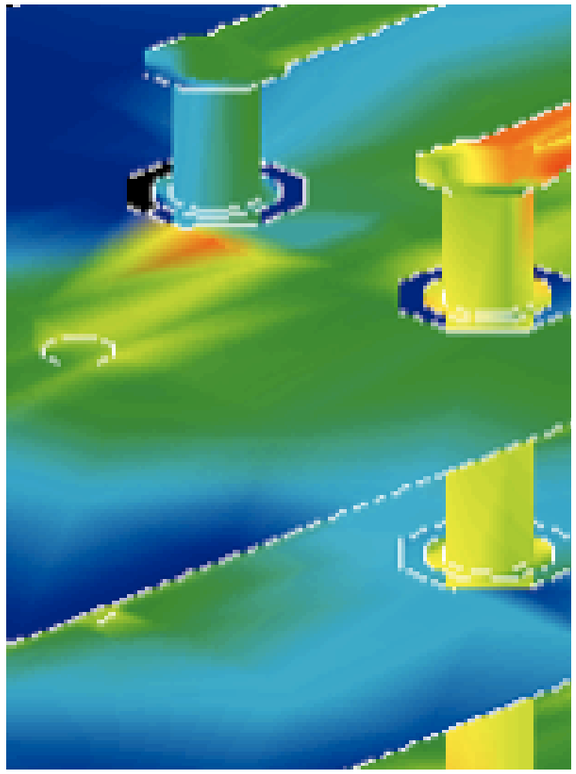
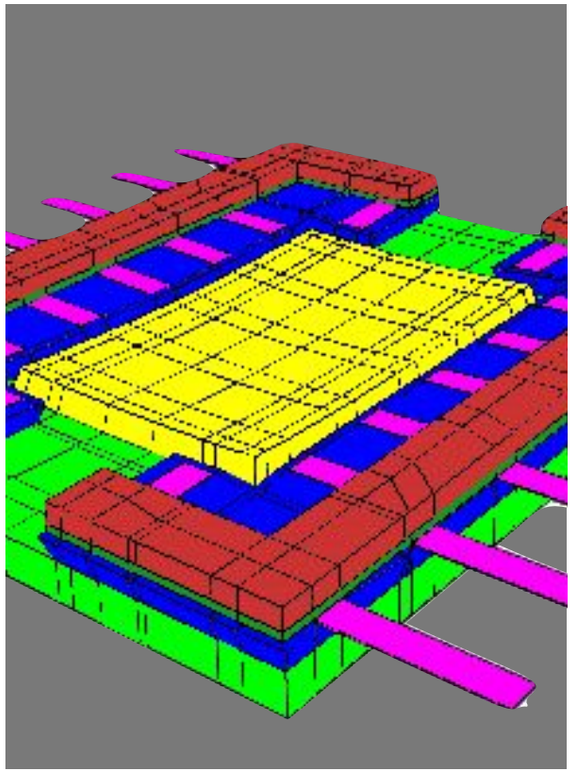
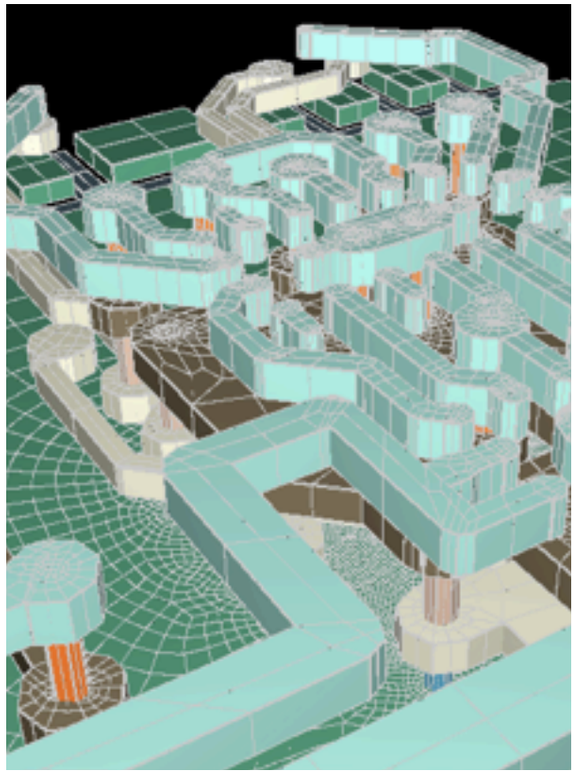








# New generation EDA tools supporting various MEMS-ASIC integration schemes

Sandeep Akkaraju

IntelliSense Corporation

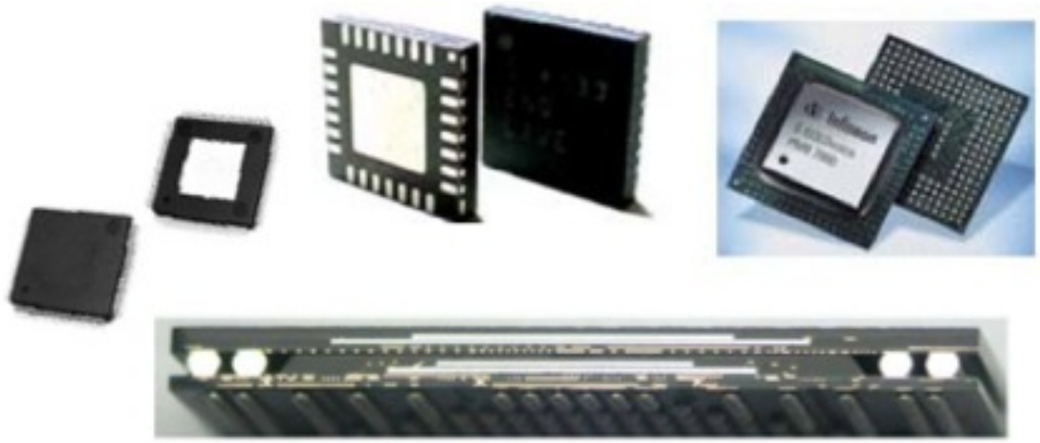
# Outline

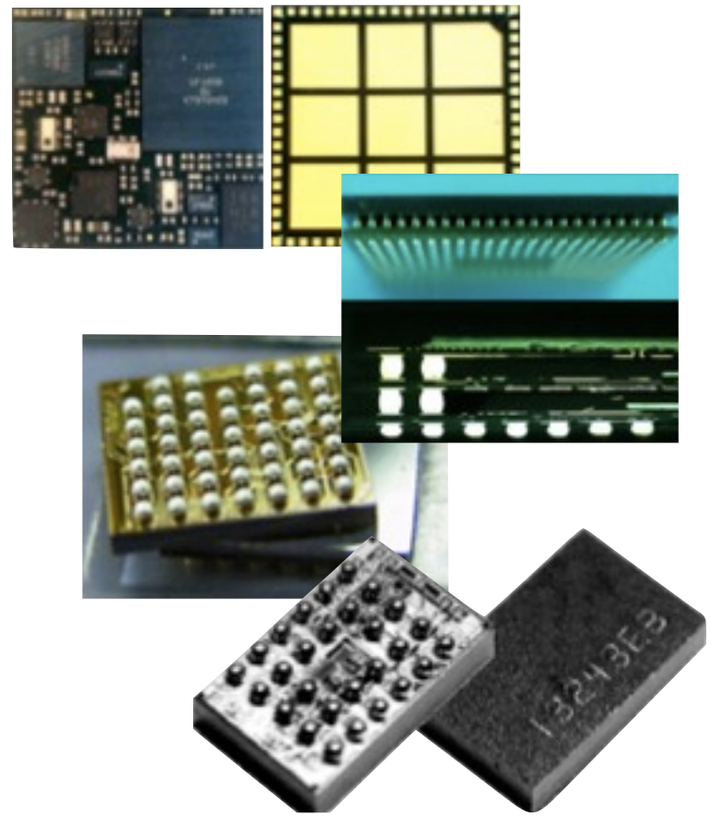
- Introduction
- Packaging impact on MEMS
- Challenges in package modeling
- Case studies
- Summary

# Introduction

# World of MEMS packaging is evolving rapidly

## Learning a new set of TLAs…





### Traditional Packaging

QFP, QFN, POP, MCM, FBGA …

### Next generation MEMS packaging

3D POP, 3D SIP, 3D WLP, 3D SIC…

## Minimum Package Volume

Pictures Courtesy ASE

# Market drivers…


## Form factor

Height & footprint (1mm going down to 0.8 mm)

## Cost

<1 $ components ⇒ low packaging BOM

## Integration

GPS + Inertial
BaseBand + Filters
Antennas + Tuners

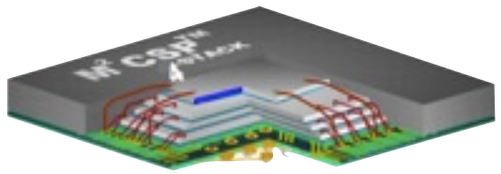
## Environment

Buzzers & bells, extreme temperatures, mechanical flexing, EM issues

## Reliability

Beyond drop tests: Fatigue, vacuum integrity, hysteresis, product year lifetime issues

# Technology drivers…



## Chipscale Packaging

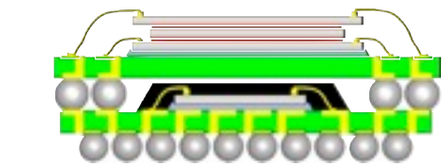
Stack large number of dies
[11 die in 1 mm form factor in 2010
14 die in 0.8 mm in 2014]

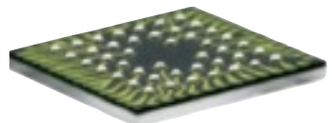
## Die/Wafer Stacking

KGD to KGSites
Direct Wafer Stacking
3D Packaging

## Via Last/Via First/TSV

Match KGD to KG sites
at high throughput

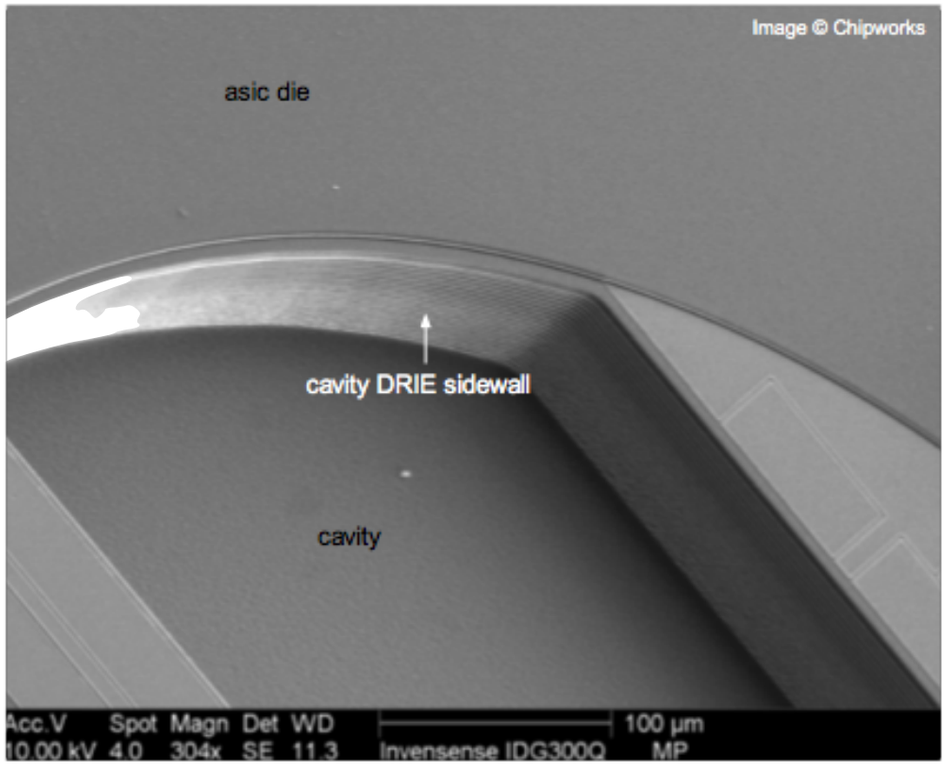


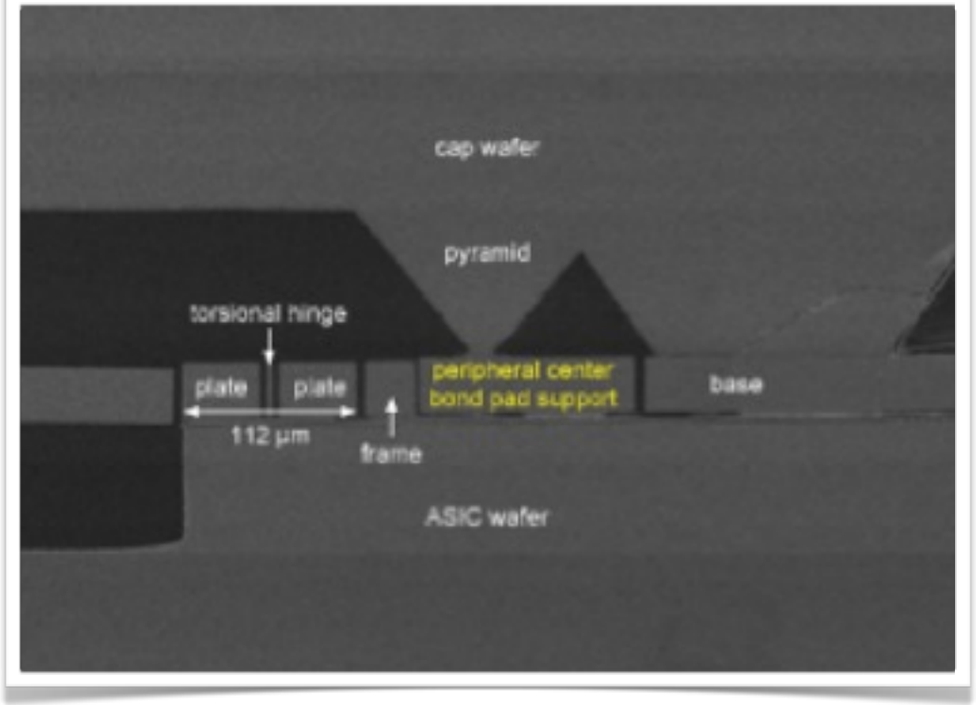


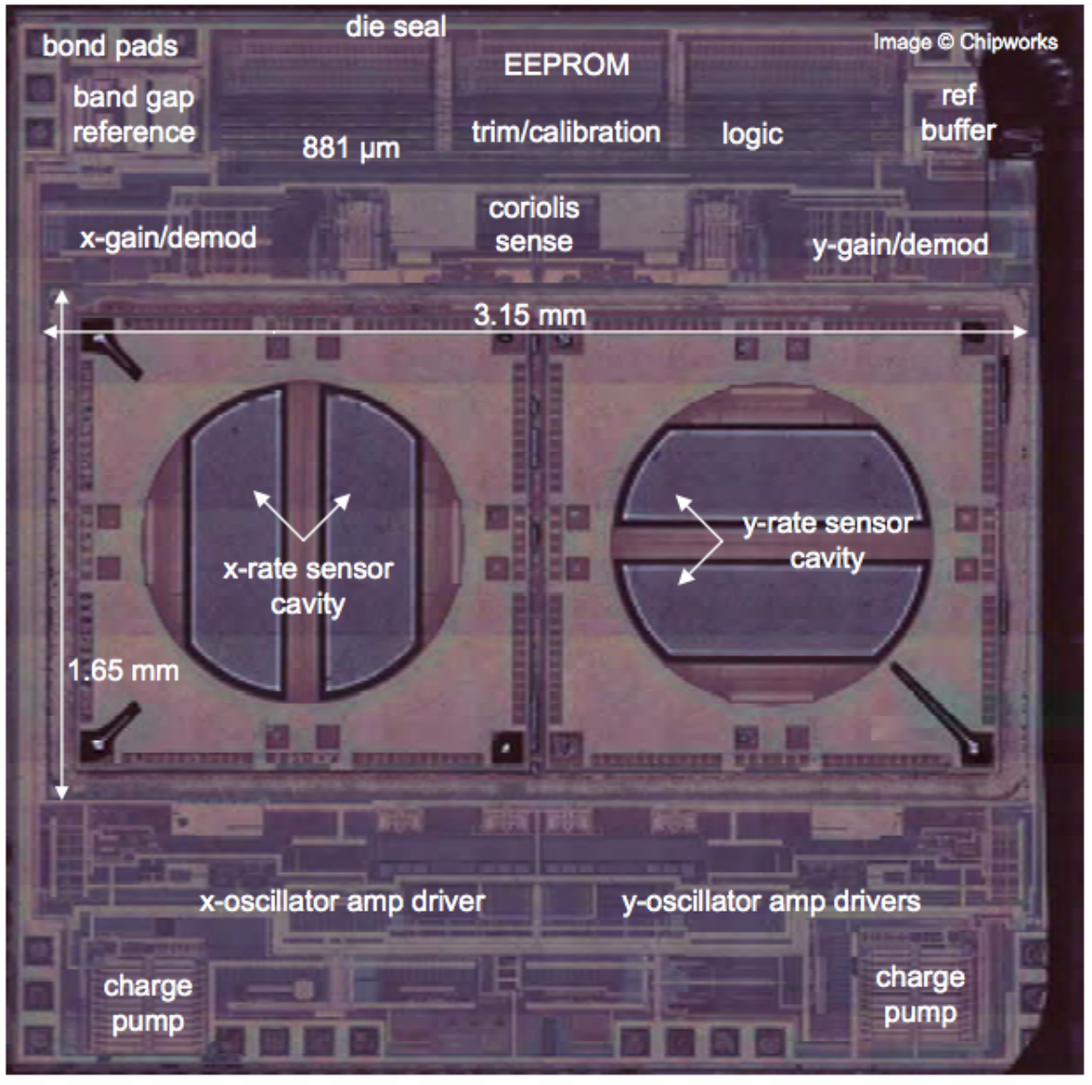
## PoP/eWLP/3DSIC/…

Package on Package
Embedded approaches

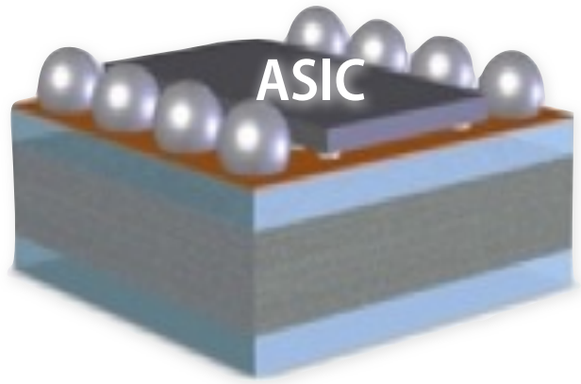
# Invensense gyro: MEMS+ASIC stacking with Al/Ge bonding

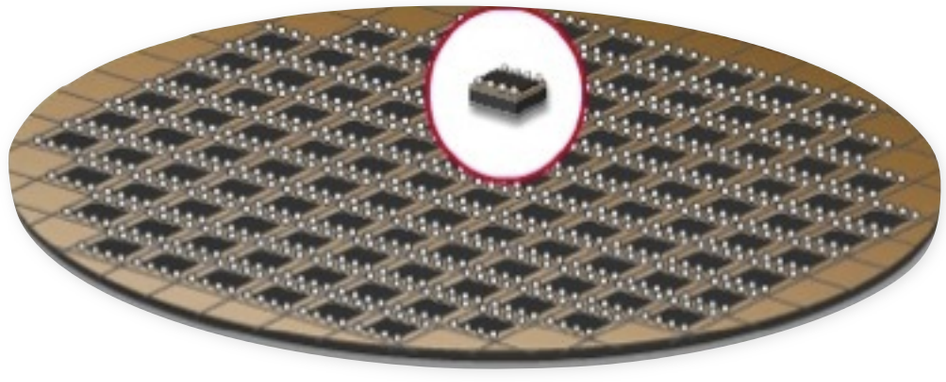


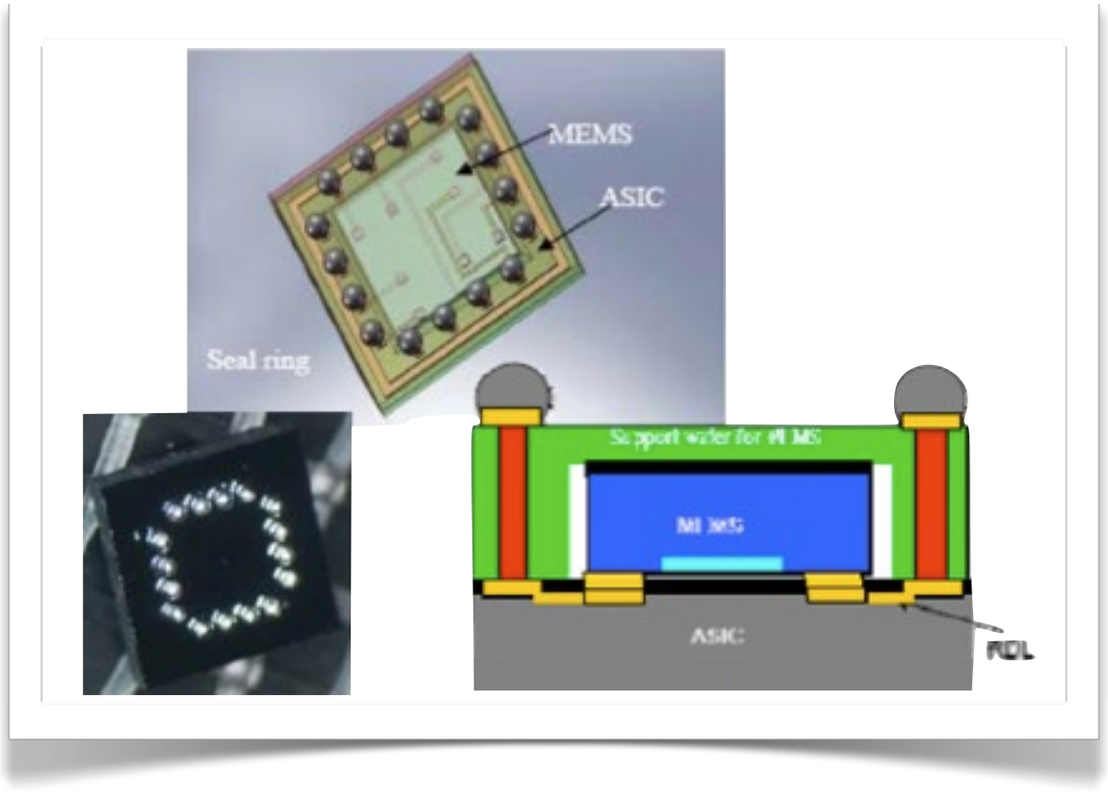
# VTI Accel: Full WLP



**Die on Wafer Assembly**
**Two level bumping**

# IME (Singapore)

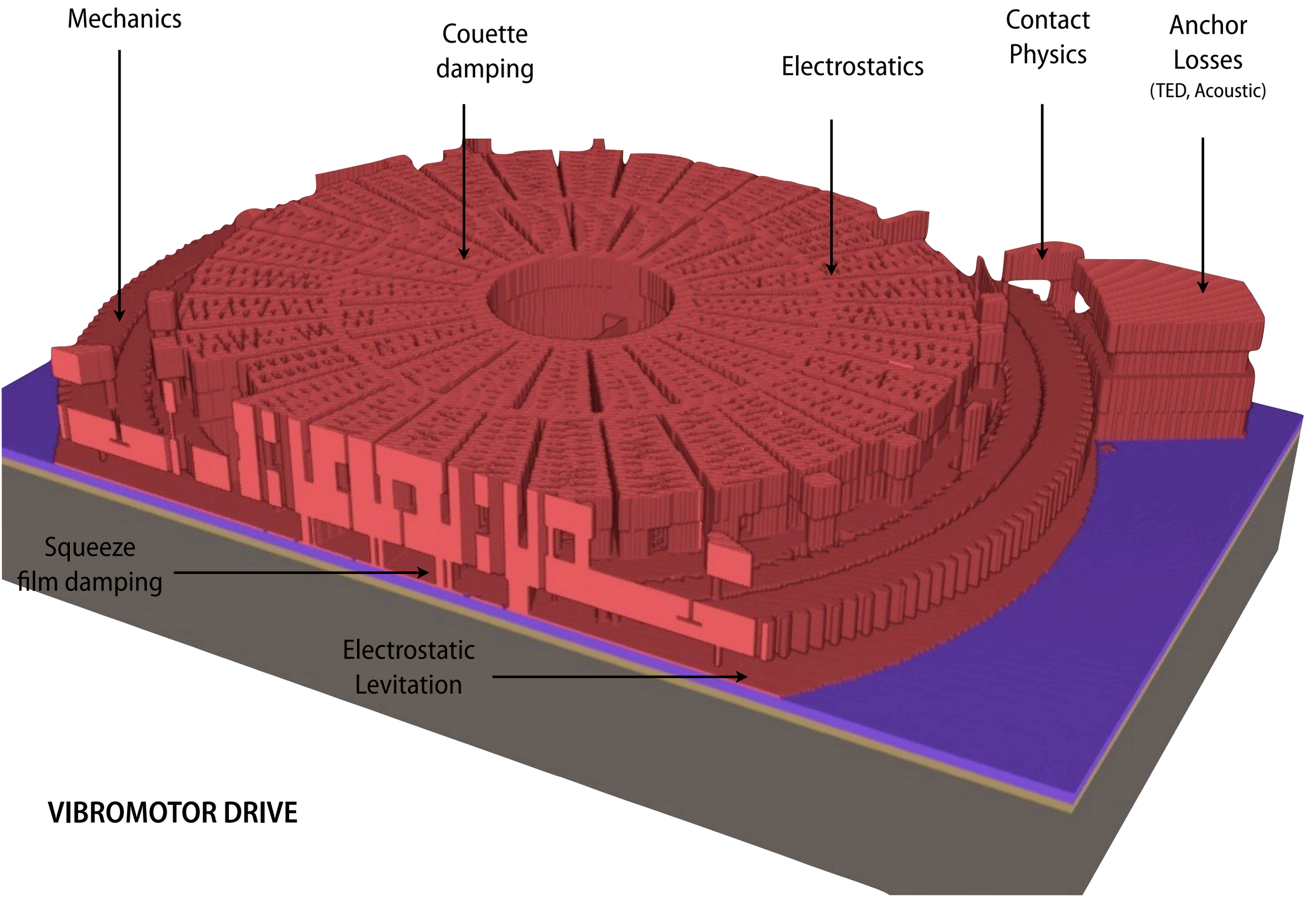



**MEMS ASIC bonding**
**Support Wafer for MEMS with bumps**

# Increasingly, MEMS is subsuming the package

# Packaging impact on MEMS

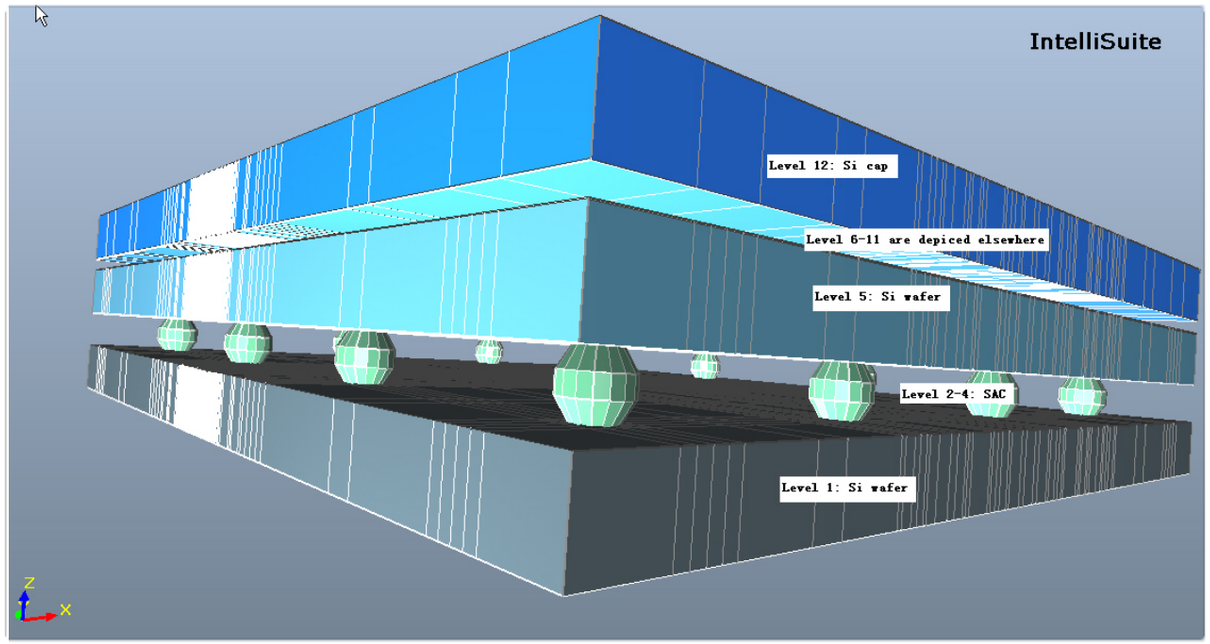
# A typical MEMS device…

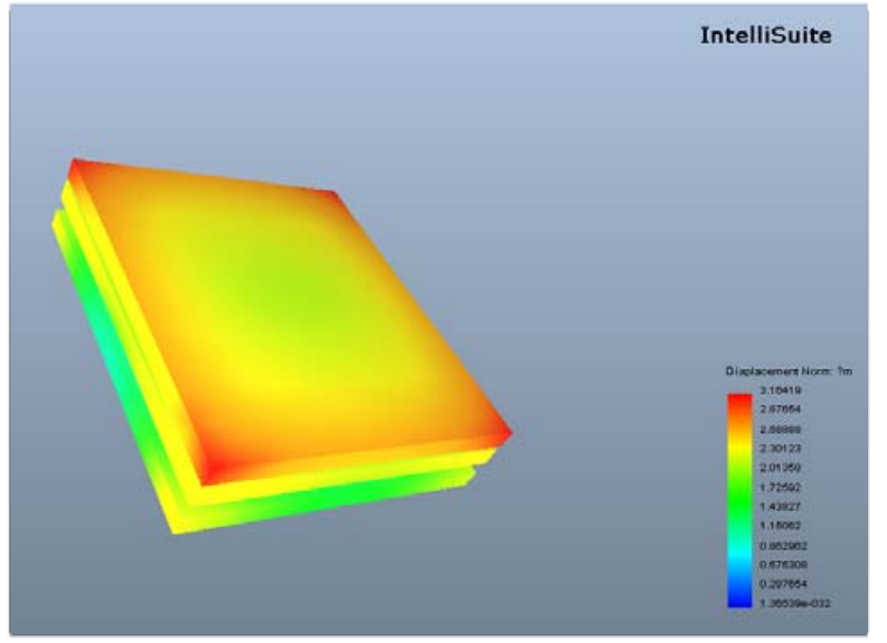



**VIBROMOTOR DRIVE**

# Now, layer packaging effects on top of this…!

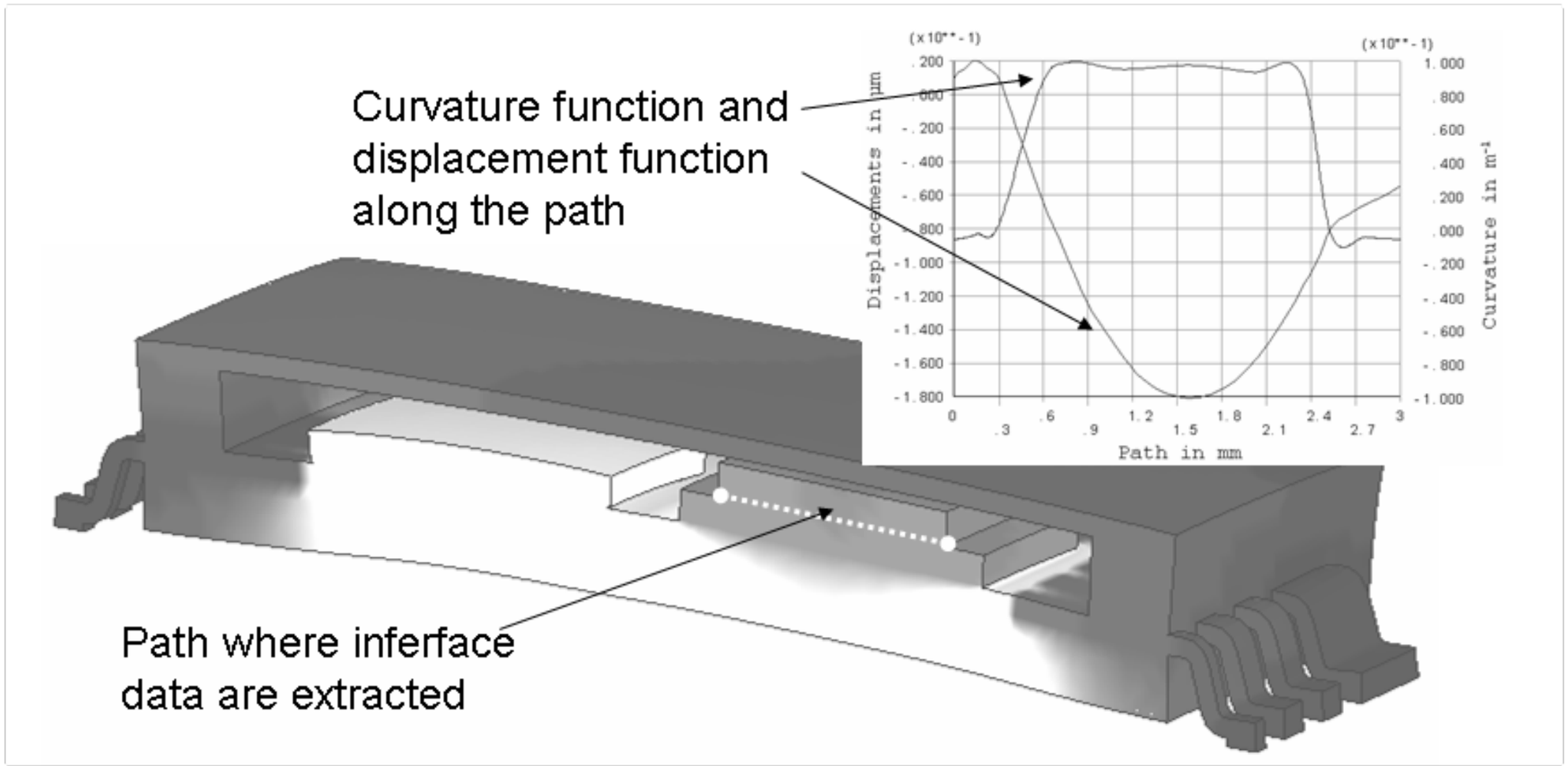
# Thermo-mechanical




**3 layer stack:**
Cap Wafer
Eutectic Bonded to Device Wafer  with TSV
Bumped to ASIC wafer
(underfill not shown)

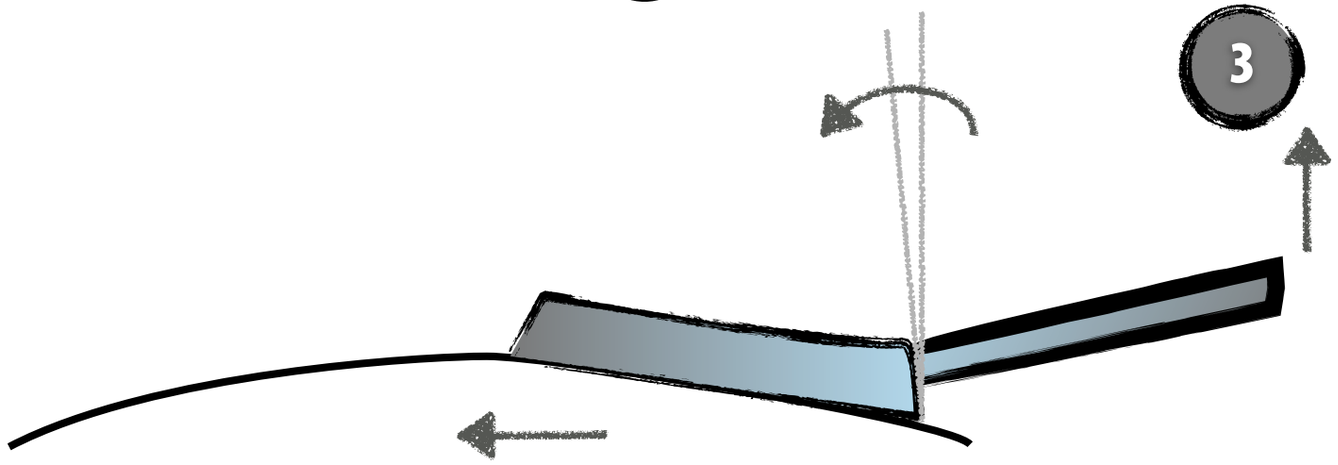
# Thermo-mechanical



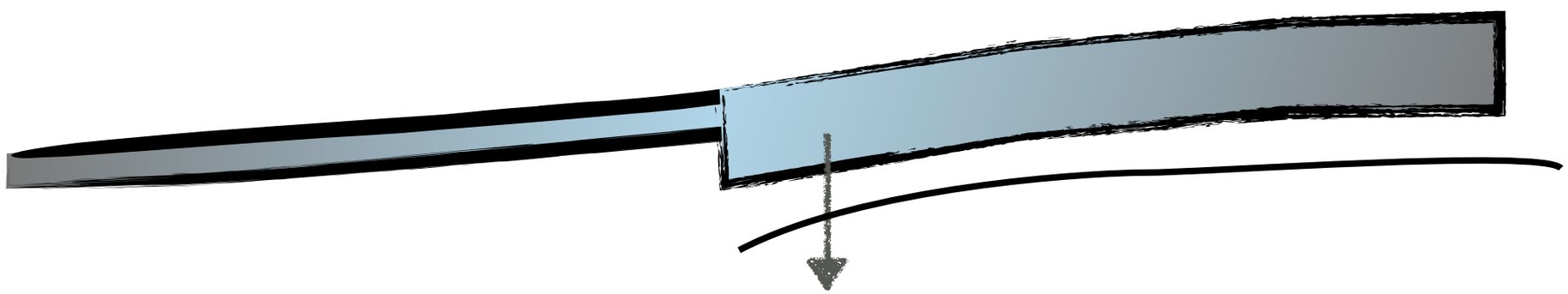
# Thermo-mechanical

2 Anchor tilt

3 Suspended mass moves up

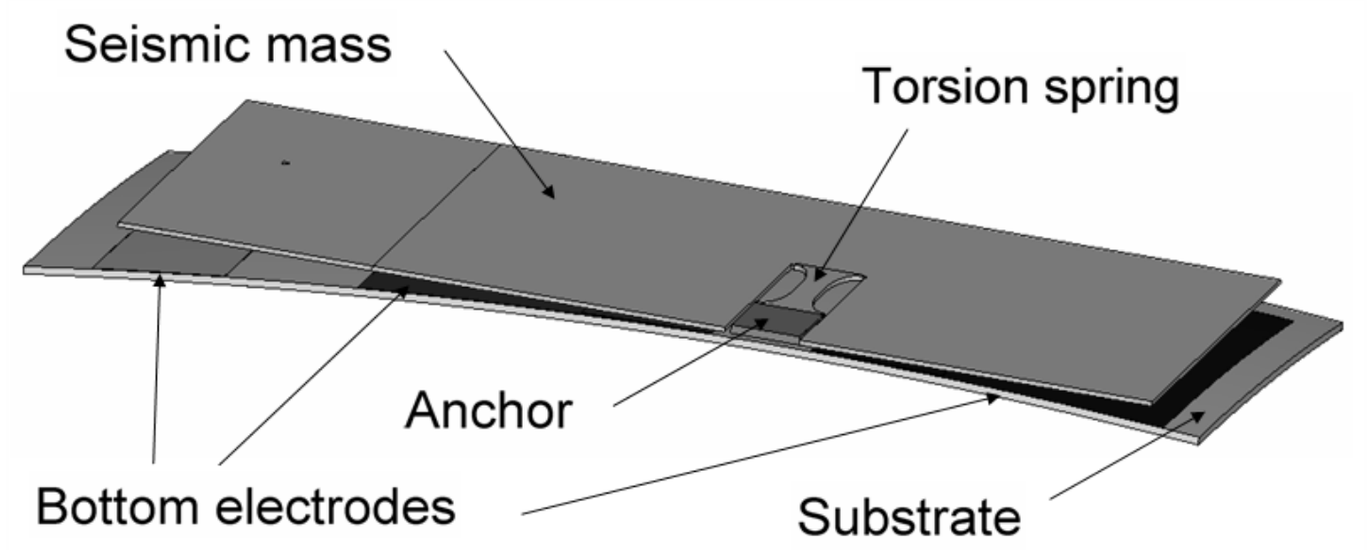


1 In-plane tensile stress

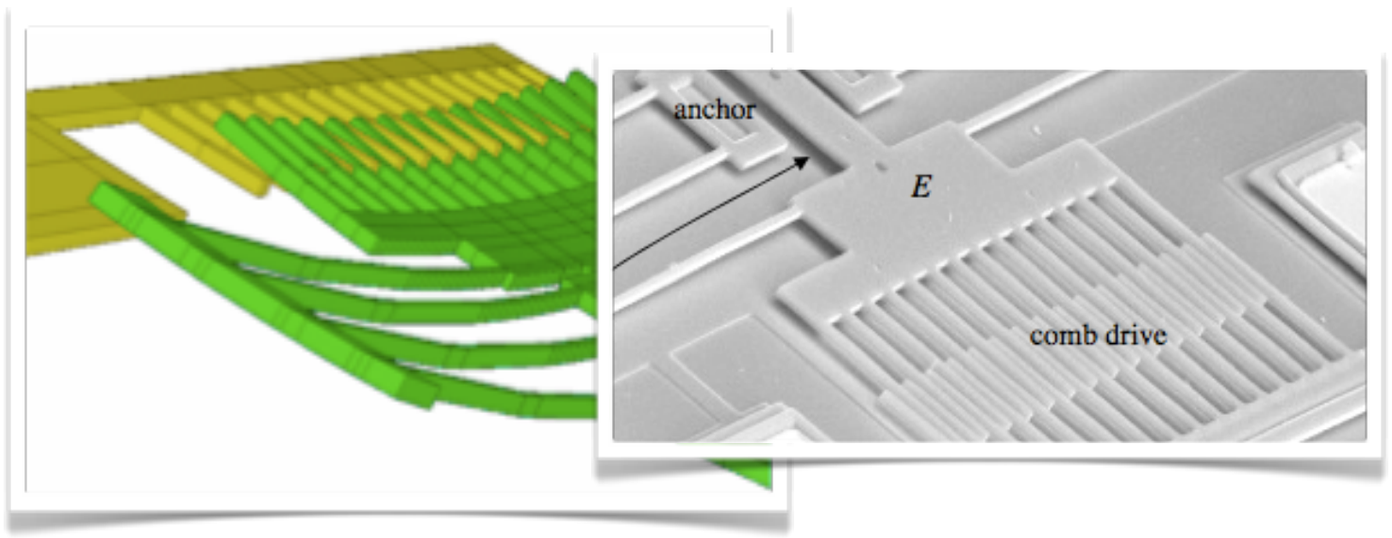


4 Suspended mass moves down

# Electro-thermal

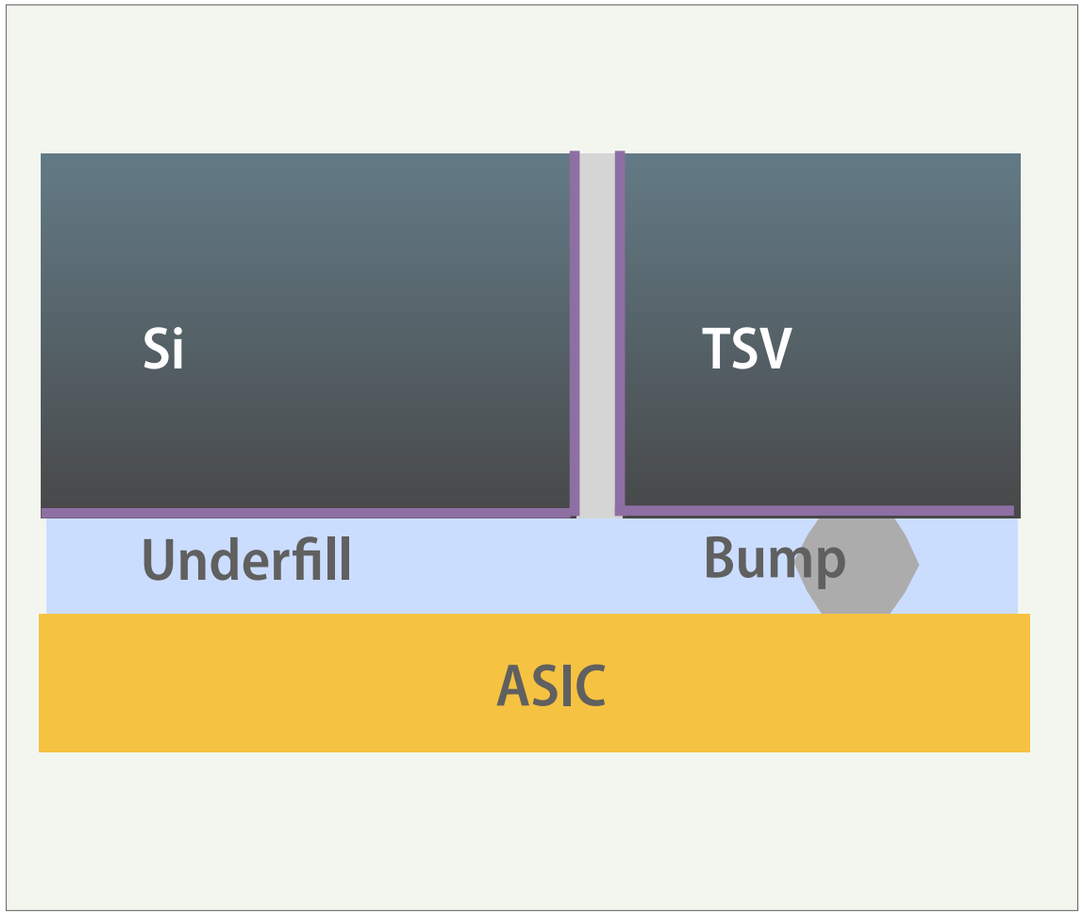



**Bottom Electrodes**
**Temperature sensitivity due to curvature**



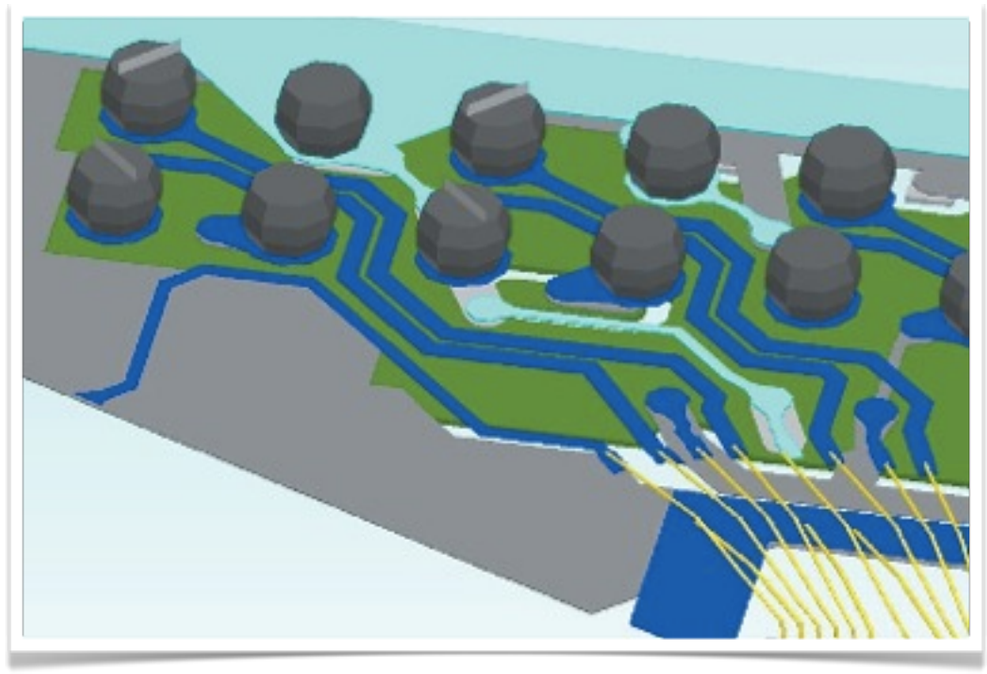

**Comb Electrodes**
**Curvature related sensitivity**

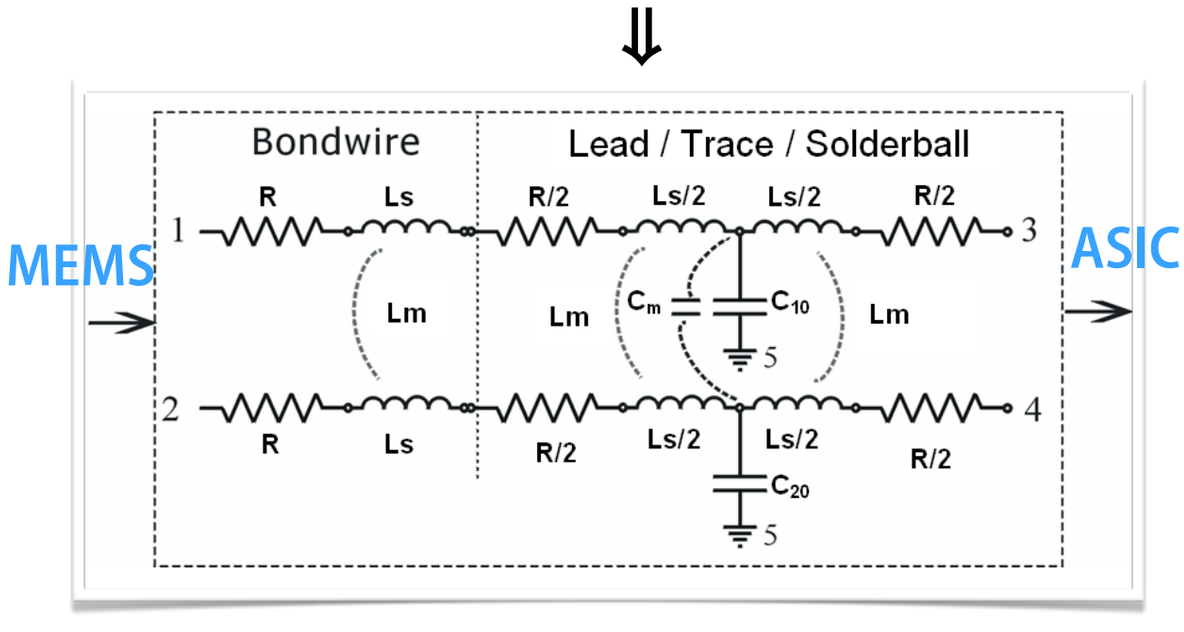
# Electrical




**Underfill dielectric increases shunt capacitance ⇒ decreased sensitivity**

Shunt issues






Parasitics & cross talk

# Packaging impact…

| | |
|---|---|
| Mechanical | Mechanical parameters: stresses, spring constants, damping, shock |
| Electrical | Sense & shunt capacitance change; pull-in and tuning voltage change |
| Thermal | Temperature co-efficients, temperature gradient co-efficients |
| Ambient | Vacuum change, viscosity change in air, moisture effects |
| Electromagnetic | Parasitic capacitances, inductances and resistance |

Manifests as bias stability, temperature coefficients, and other performance killers…

# Challenges in package modeling

# MEMS Design Is A Collaboration Challenge…

Program Manager

System Architect

Device Engineer

Process Engineer

# THE CHAIN OF PAIN...

Manufacturing Engineer

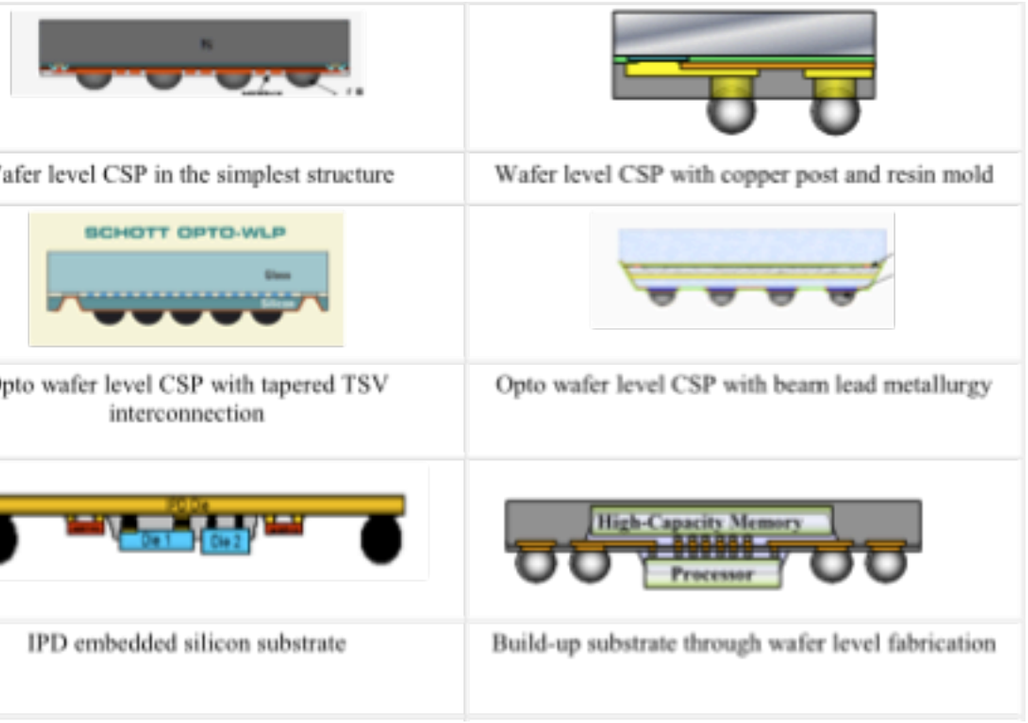
Test Engineer

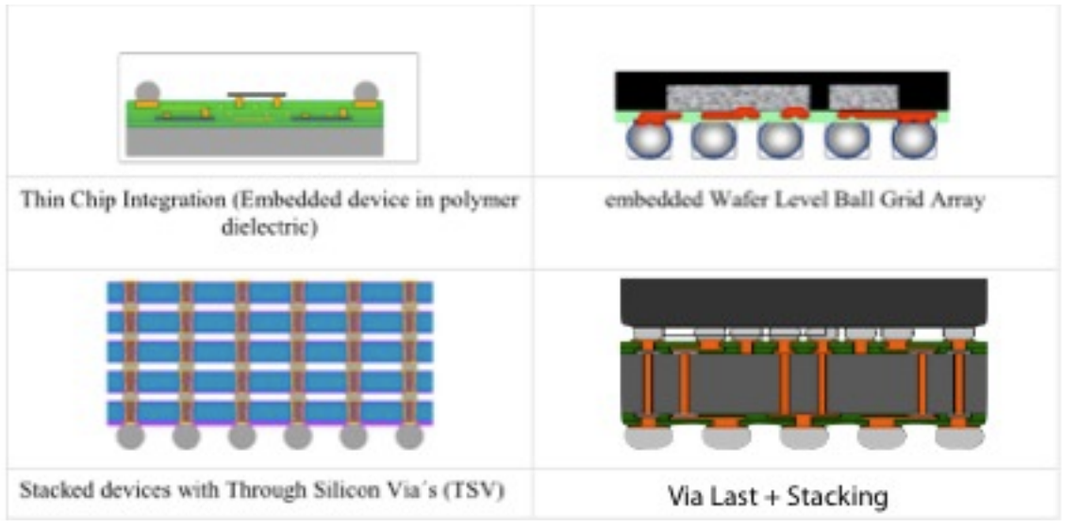
Packaging Engineer

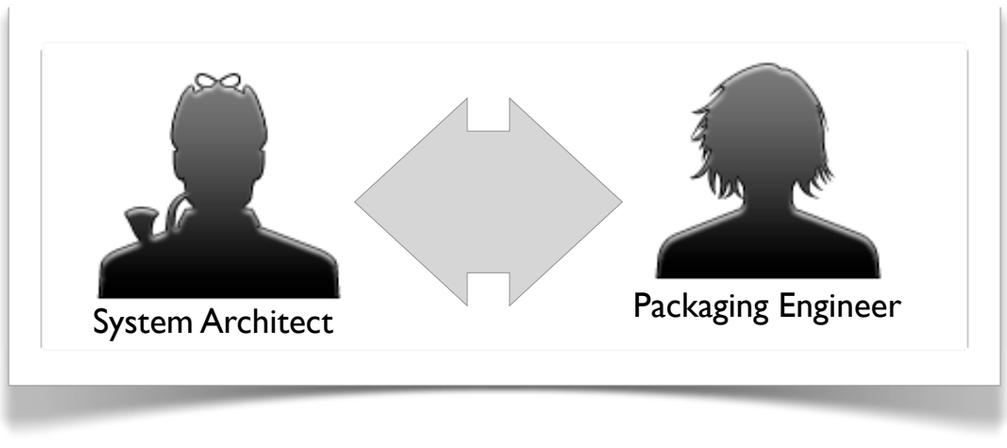
Electrical Engineer

# The chain of pain… (1)

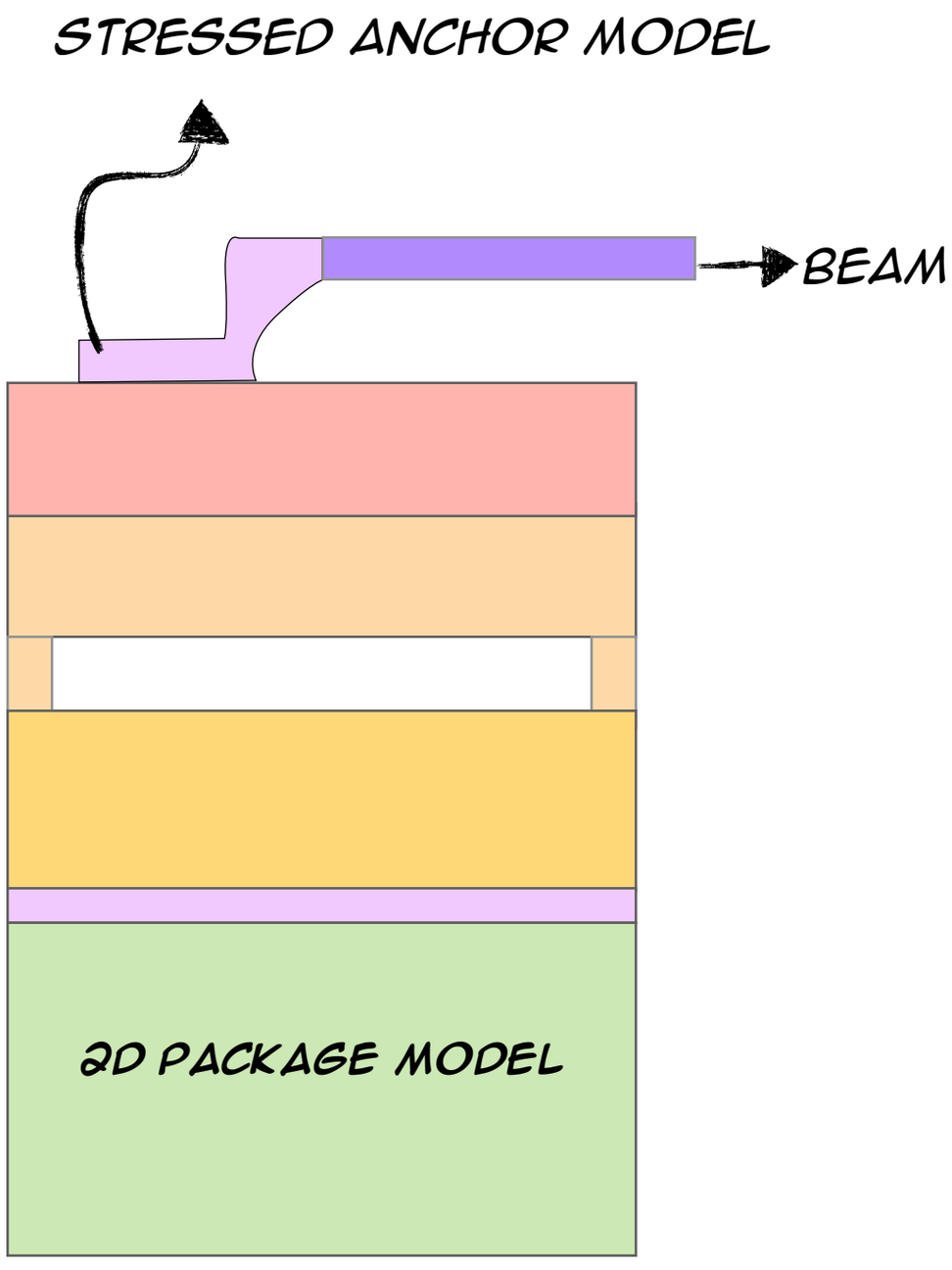
## How do you explore a huge range of packaging options?

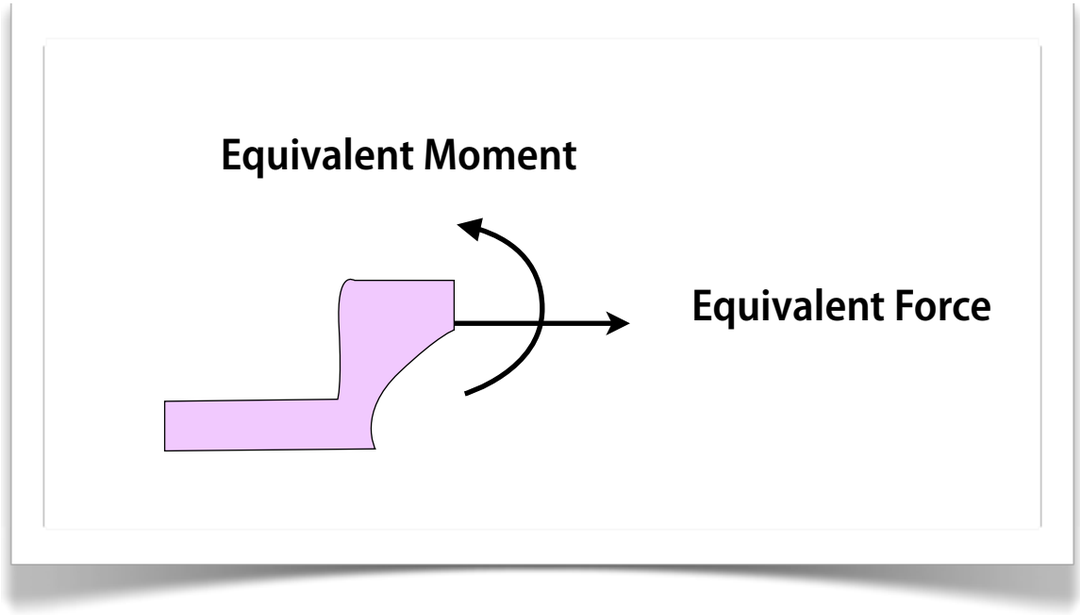


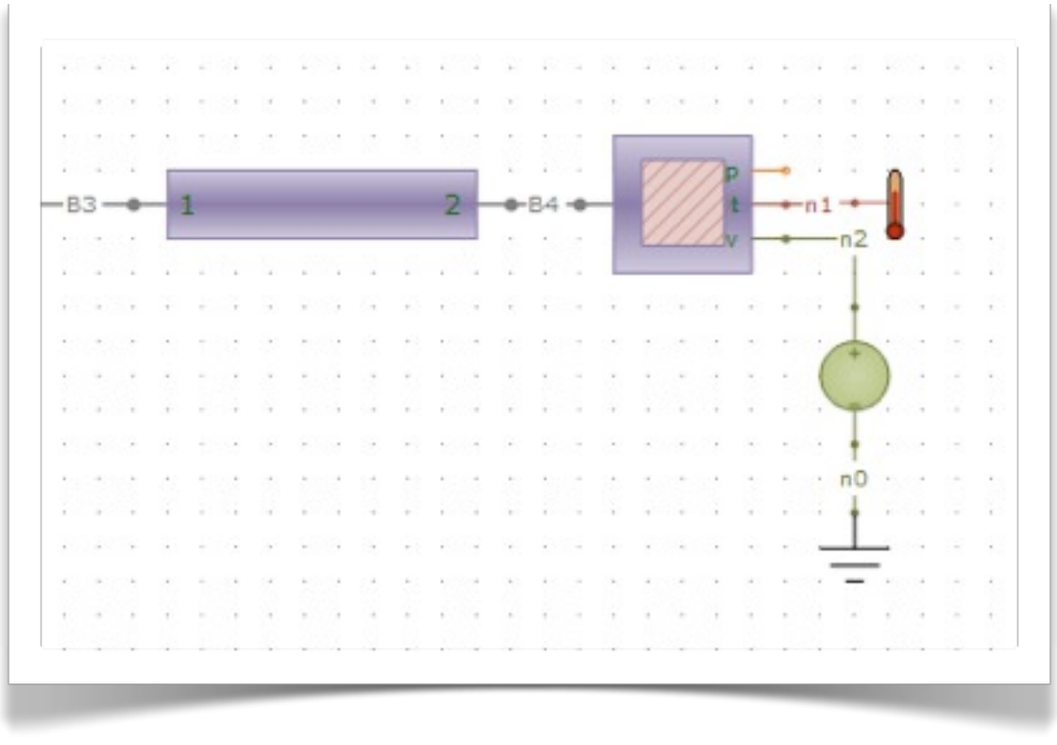



# Compact models for packaging…



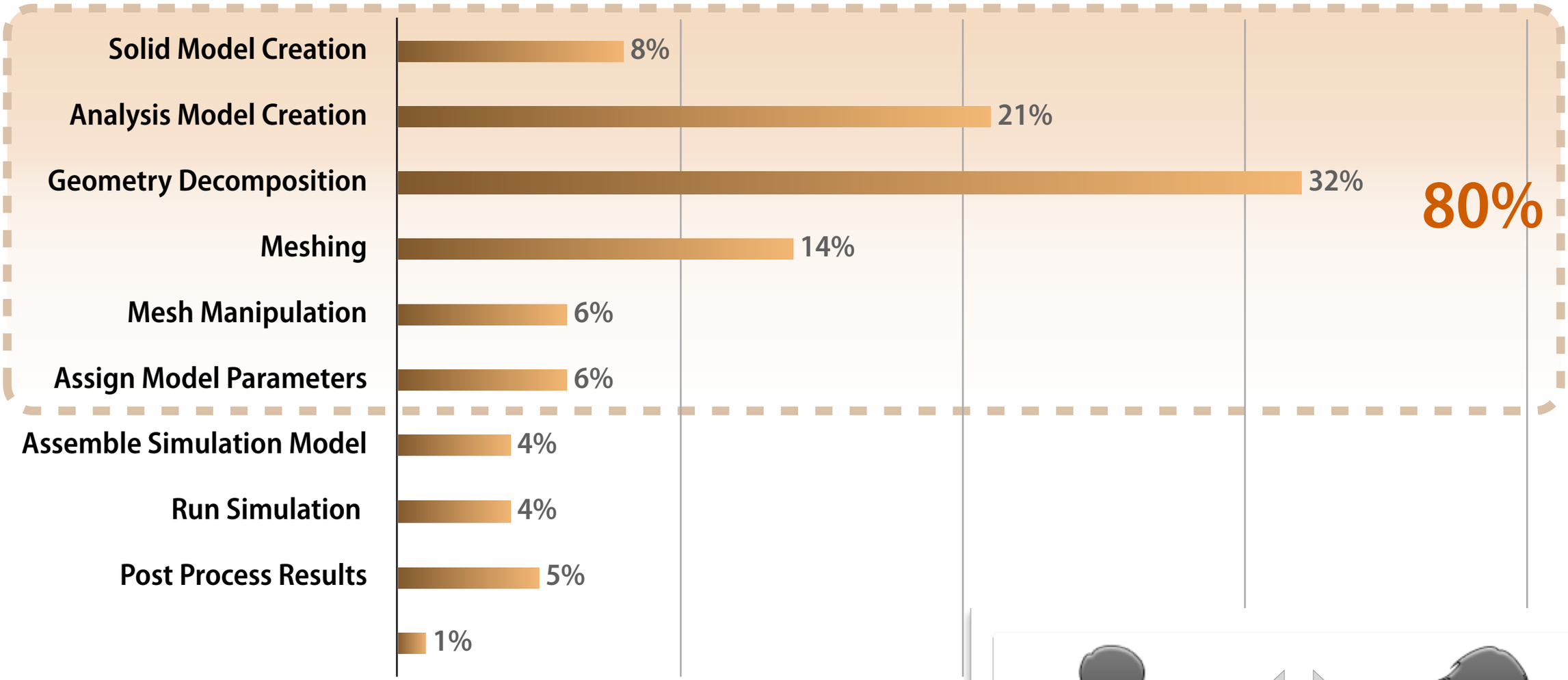



# The chain of pain… (2)

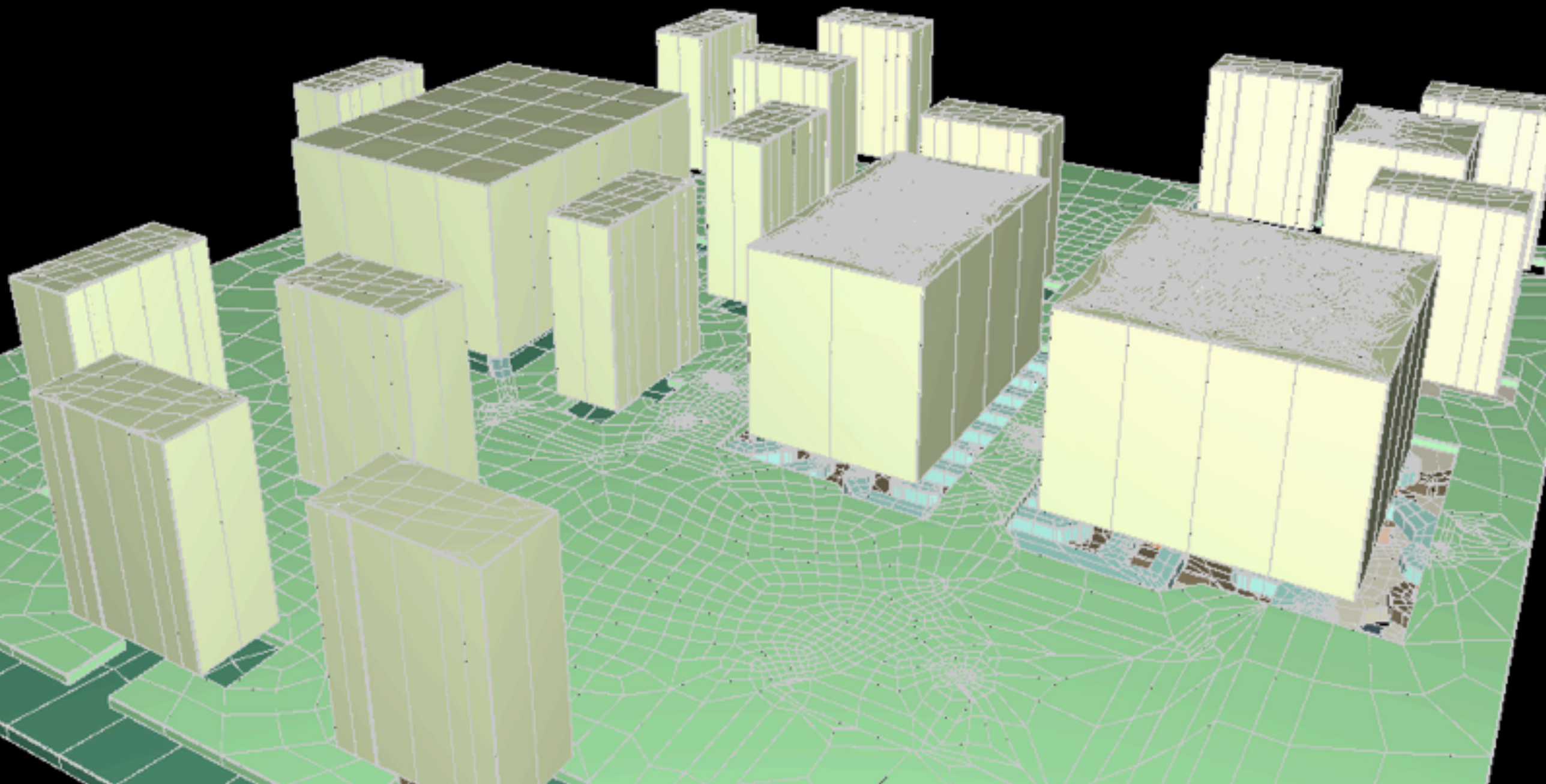
## How do you efficiently create MEMS + Package models?

Close to 80% of the time spent in mesh creation and manipulation…

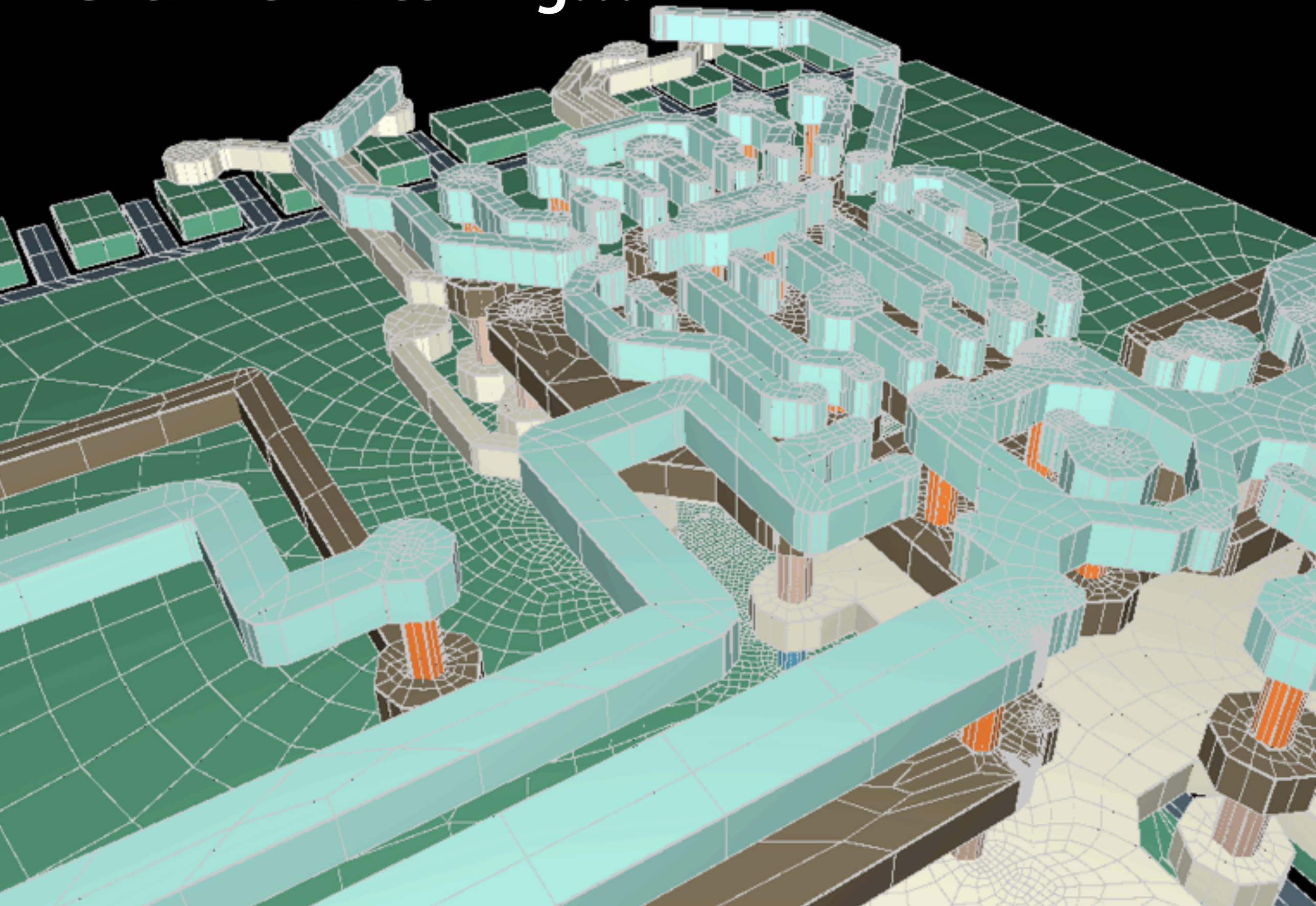



Courtesy: Matt Staten, Computing and Modeling Dept, Sandia National Labs

# Automated HEX meshing…

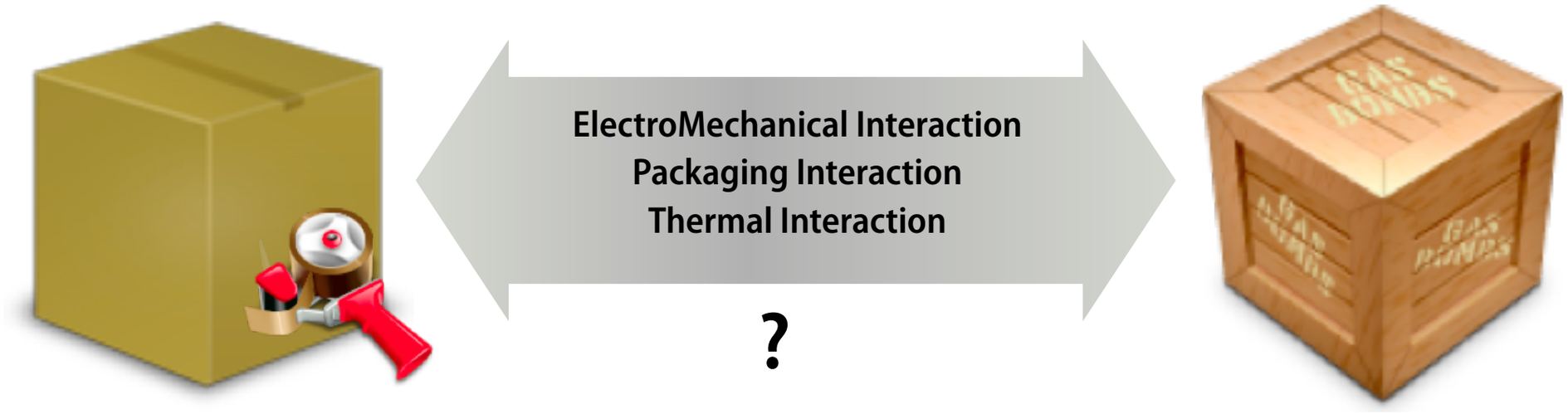


# 1 Click Hex Meshing…



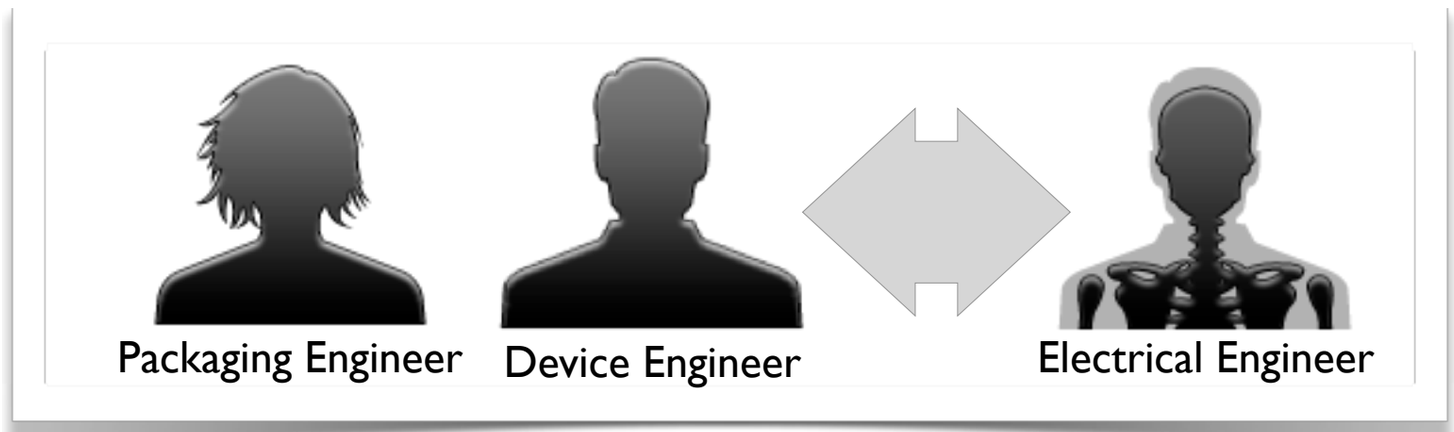
# The chain of pain… (3)

How do you compensate packaging and temperature effects?




**MEMS+Package**

**ASIC**

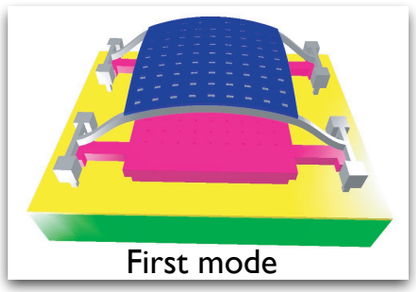


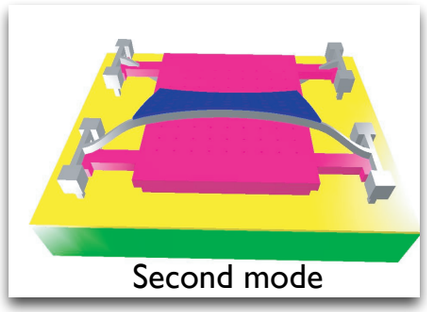
# Automated System Model Extraction (SME)

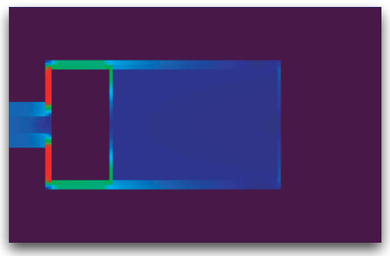
Capture strain energy associated with each mode

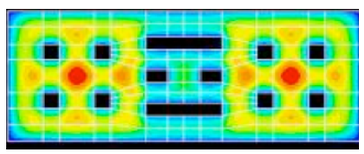
Capture electrostatic energy associated with each mode

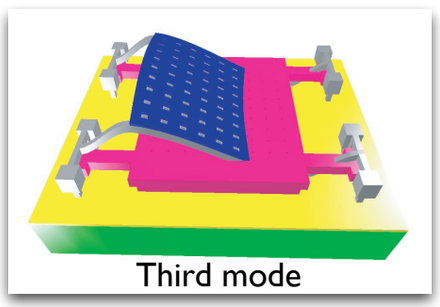
Capture fluid damping characteristics

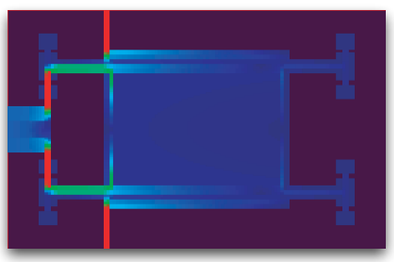






Arnoldi/Krylov sub-space reduction


N-DOF behavioral model based on Lagrangian formulation

$$\frac{d}{dt}\left(\frac{\partial L}{\partial q_j}\right) - \frac{\partial L}{\partial q_j} = 0$$

Compact Representation

HDL

Hardware Description

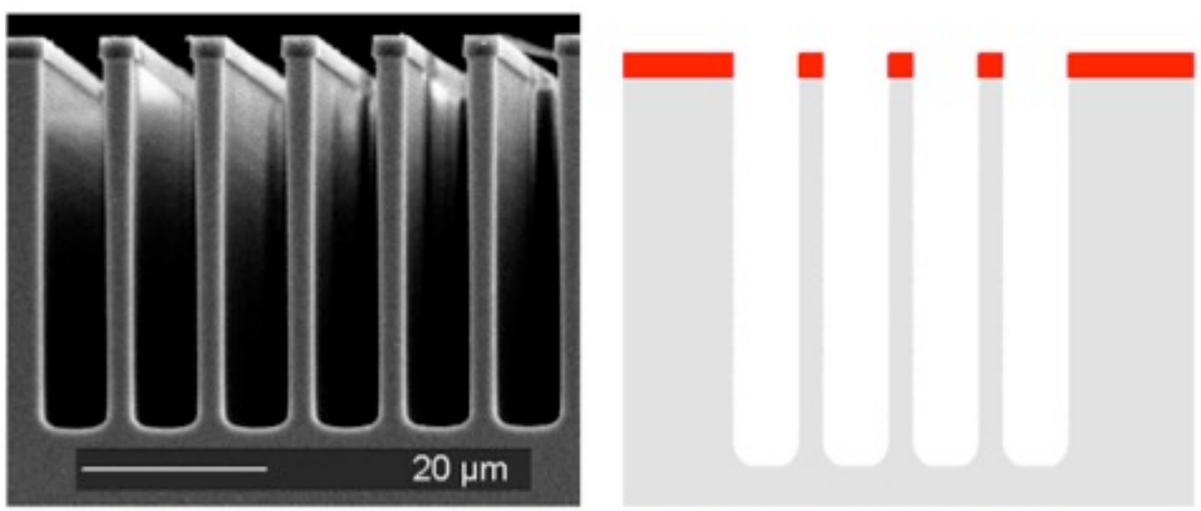
❶ Capture total energy of relevant mode (Mechanical, Electrostatic, Dissipation)

❷ Krylov/Arnoldi methods to generate Lagrangian formulation

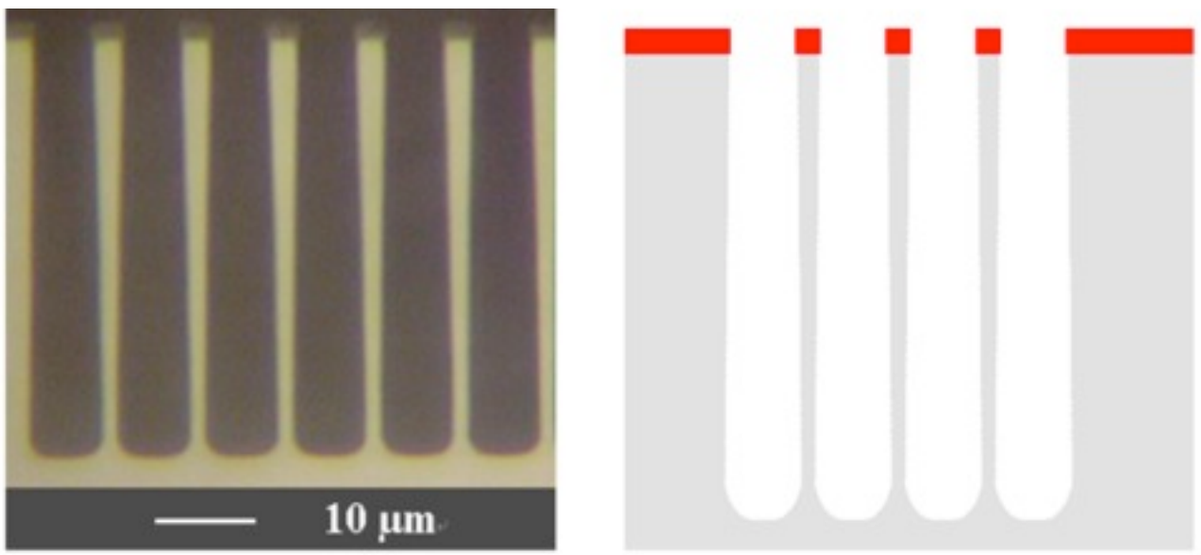
❸ Create Compact model for system modeling

# The chain of pain… (4)

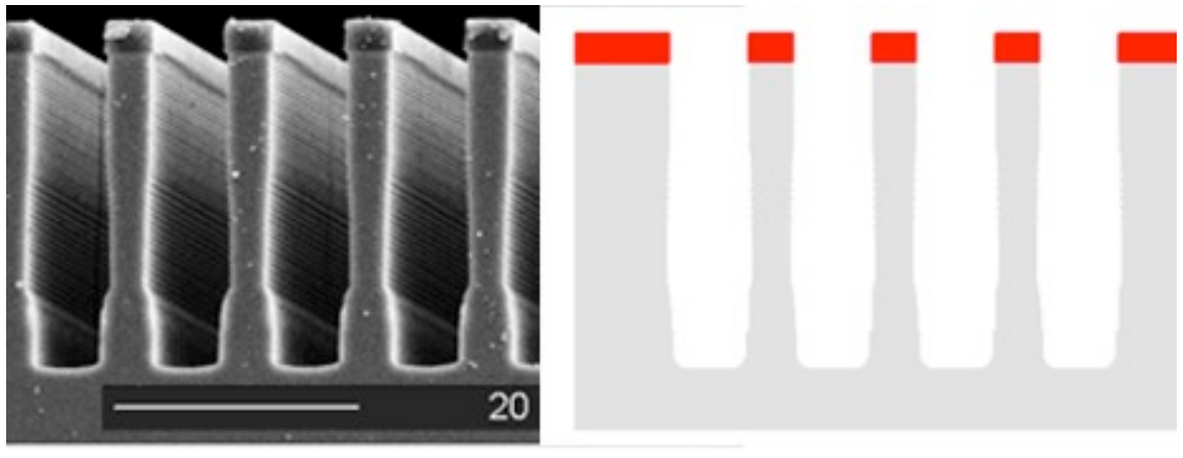
## How do you fine tune TSV processes?




The experimental results of the etching. Comparison of etching 5 µm openings with an etch/dep cycle of 7s/7s.




Comparison of etching a 5 µm trench with a 7s/8s cycle

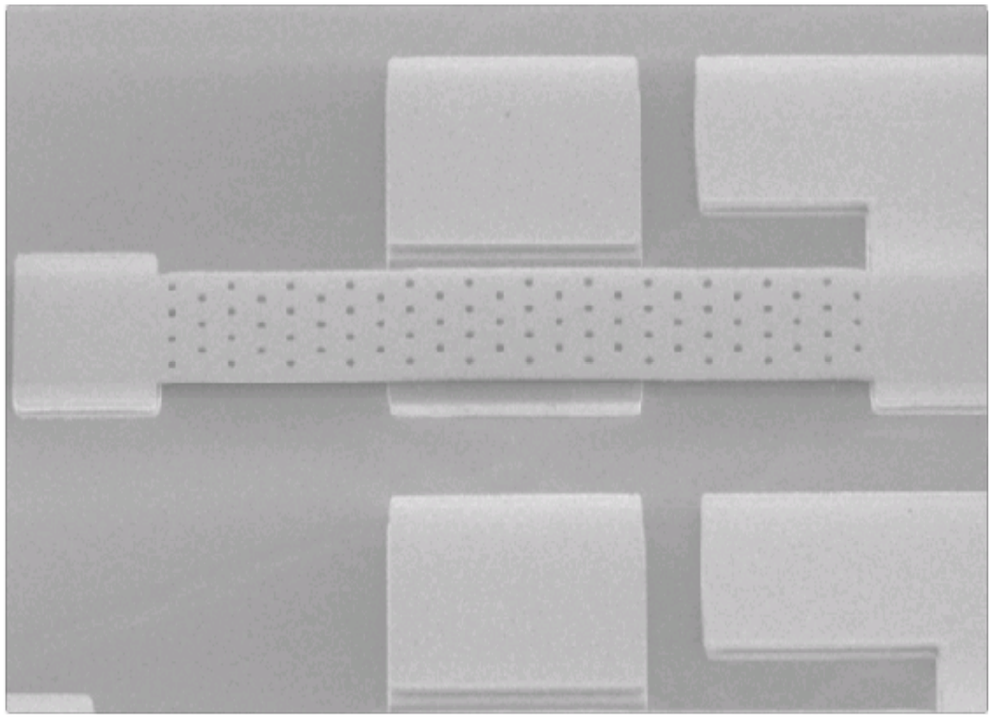



The experimental result of the etching of trenches using three etching steps with different etching/polymerization time configurations. 7s/7s, 9s/7s and 5s/7s are used sequentially, each for 5 minutes.

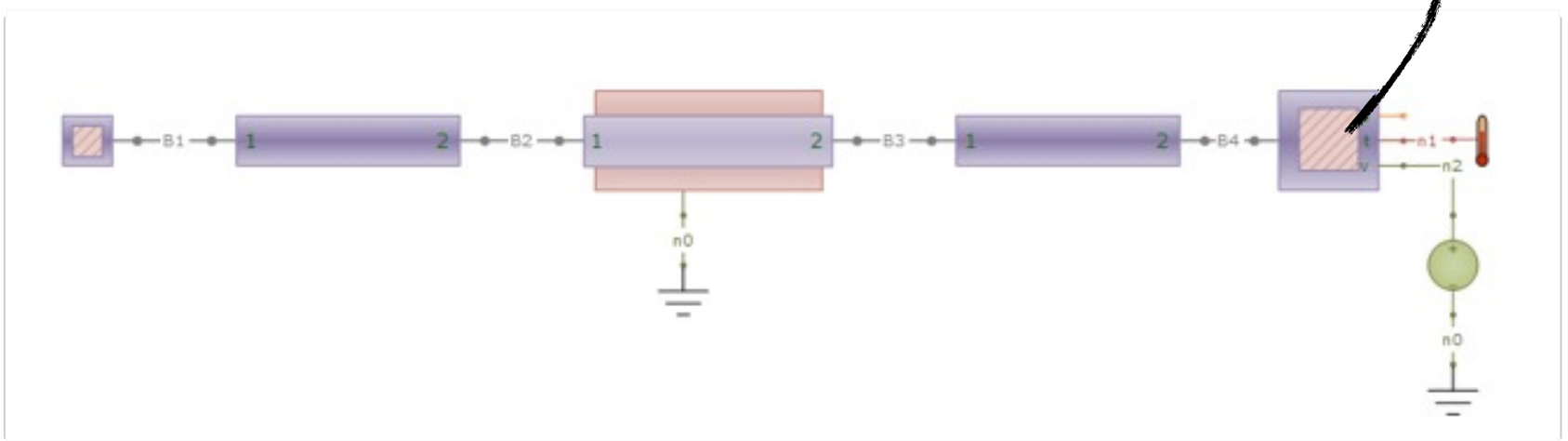
Process Engineer

# Case Studies

# Northrup: RF Switch

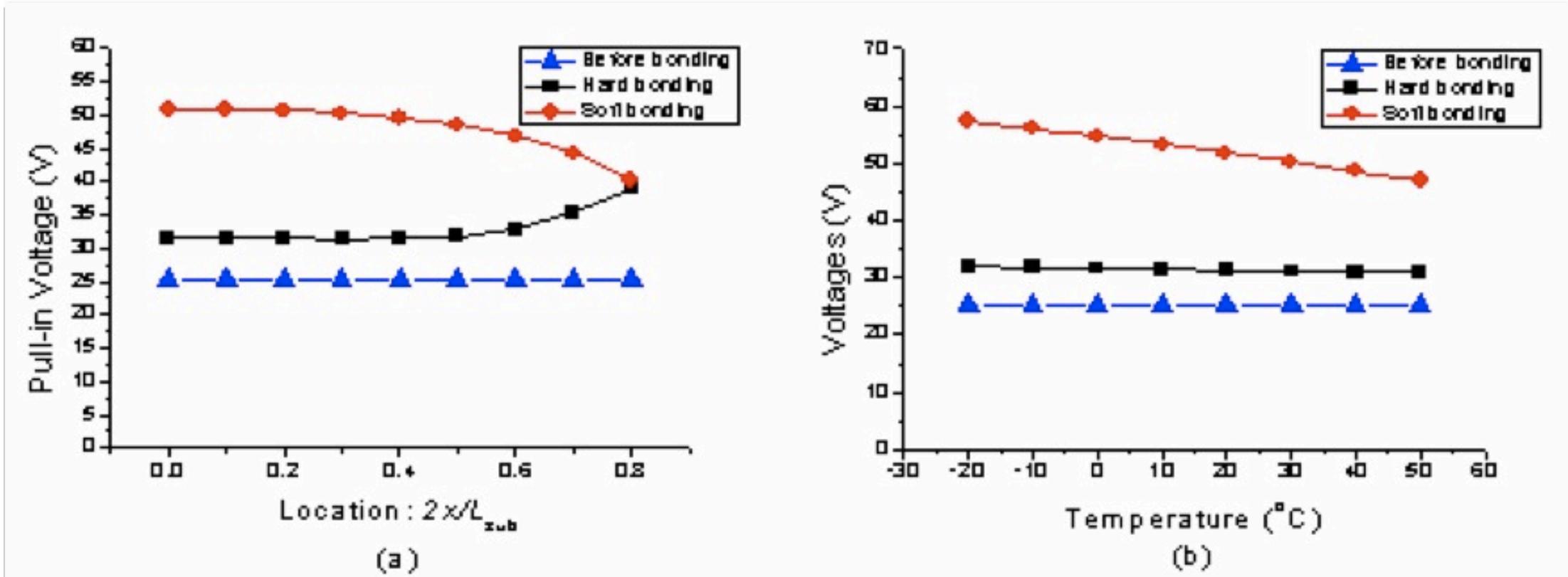


**Stressed Anchor Model**



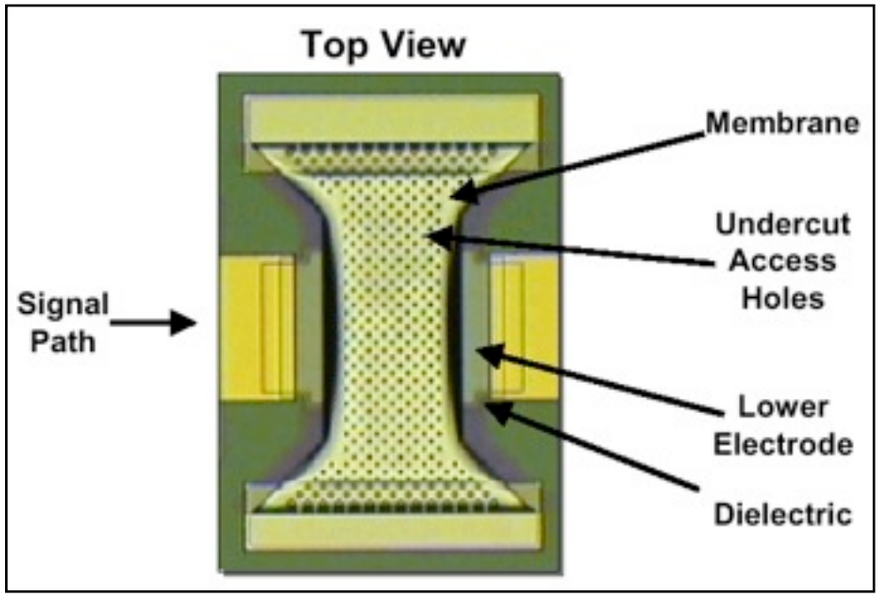
# RF Switch

Within 10% of full FEA models…

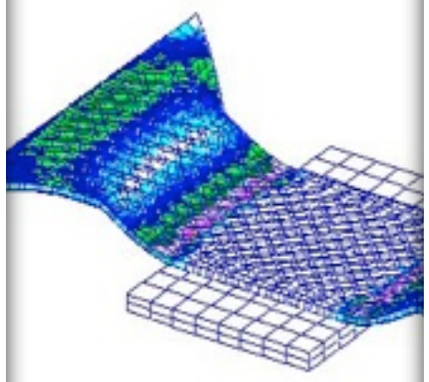



**Hard bonding**: Au-Si Eutectic on Ceramic Substrate
**Soft bonding**: Epoxy bonding on FR-4

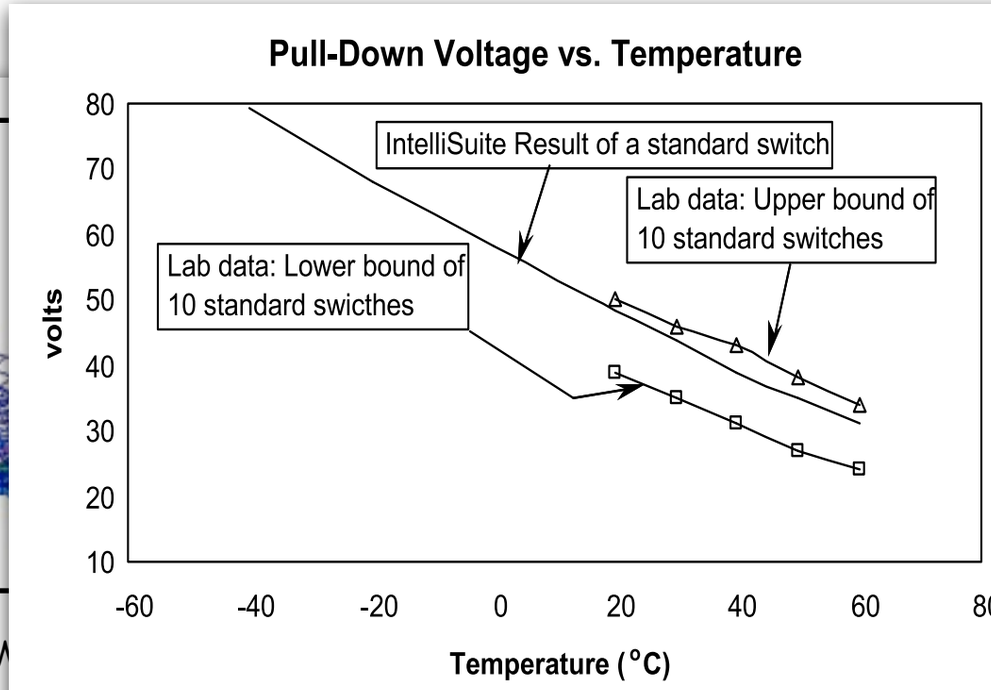
# Raytheon RF Switch




SEM AND DEVICE CONFIGURATION

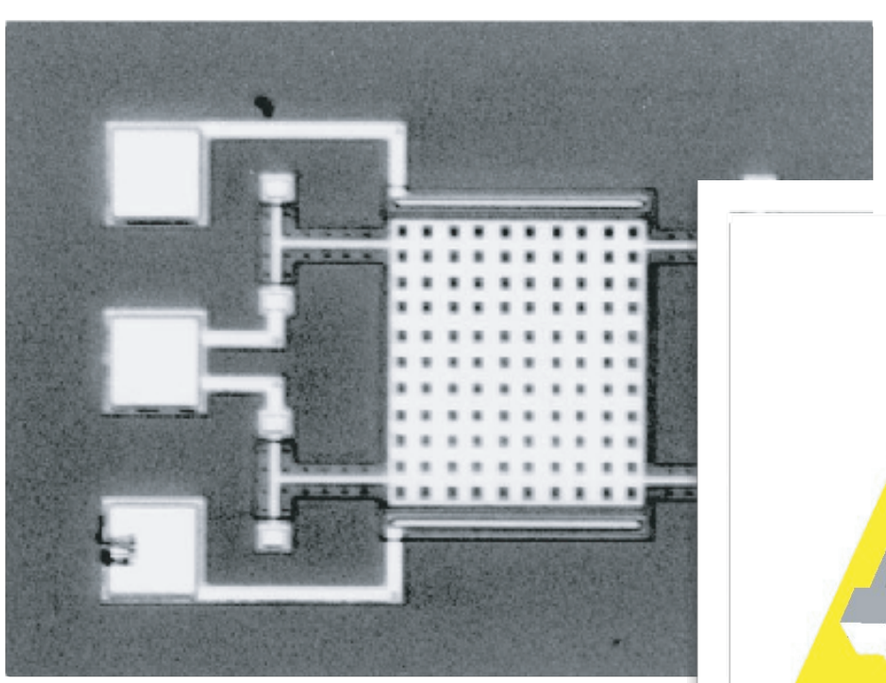


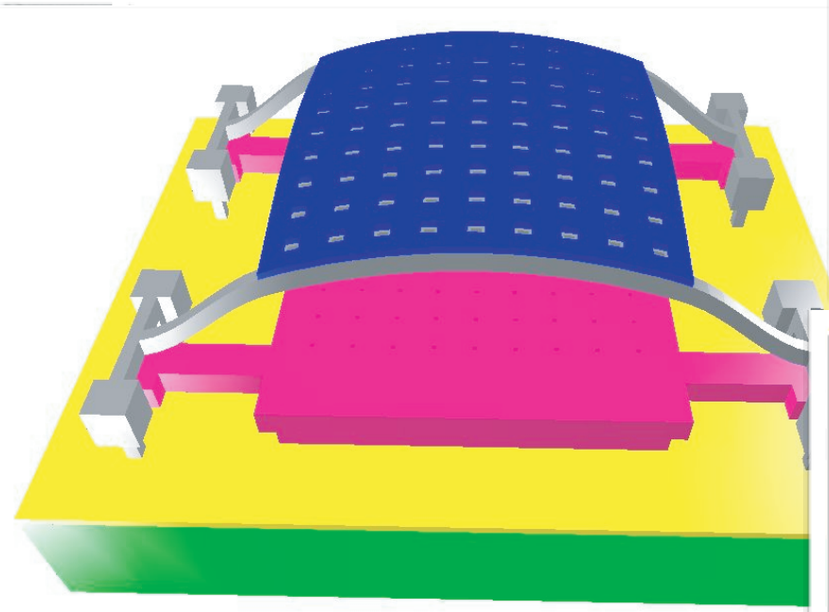
NTACT ANALYSIS VON M



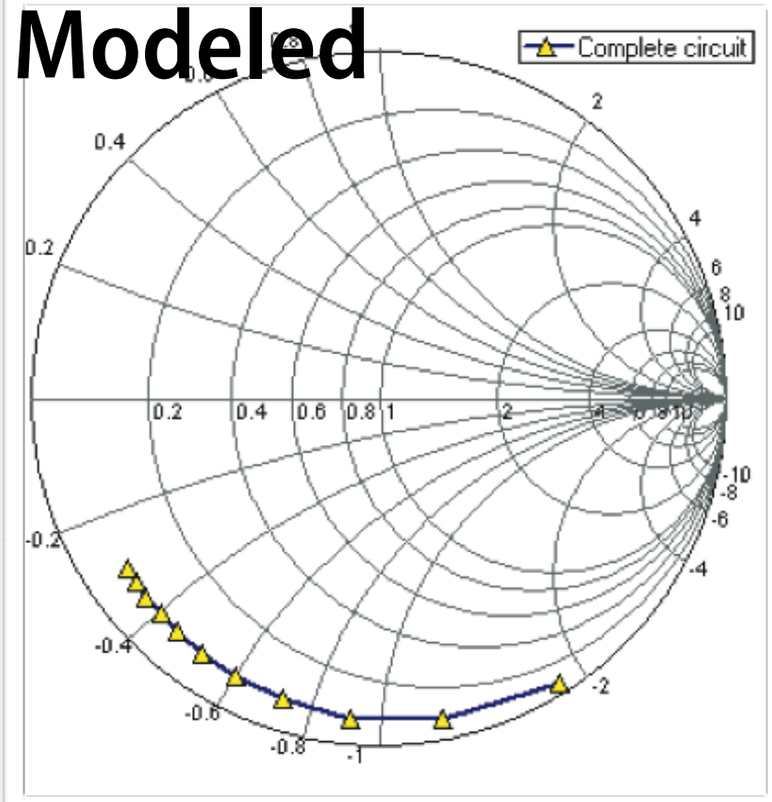

PERFORMANCE OF SWITCH

# Tunable capacitor

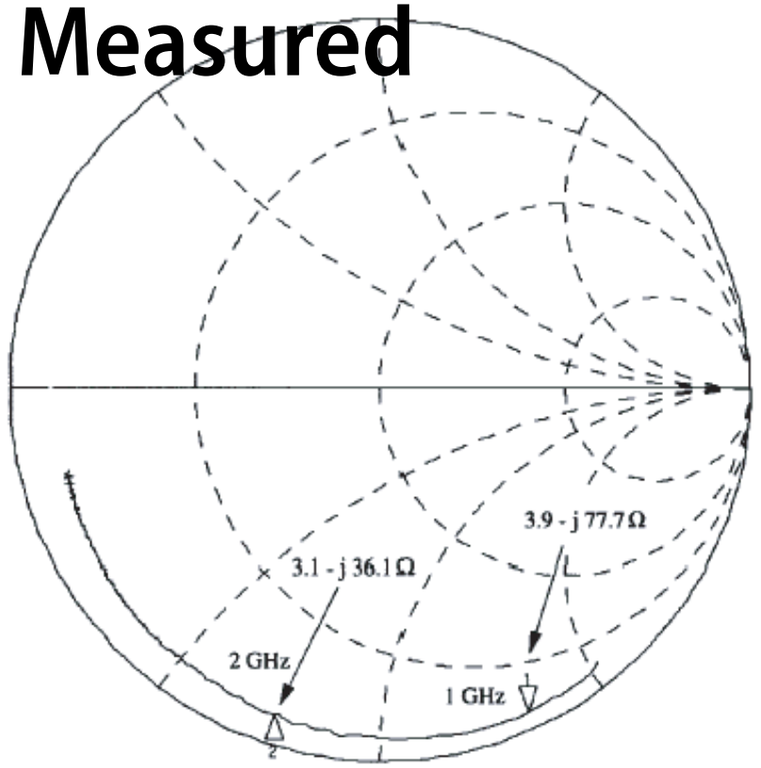




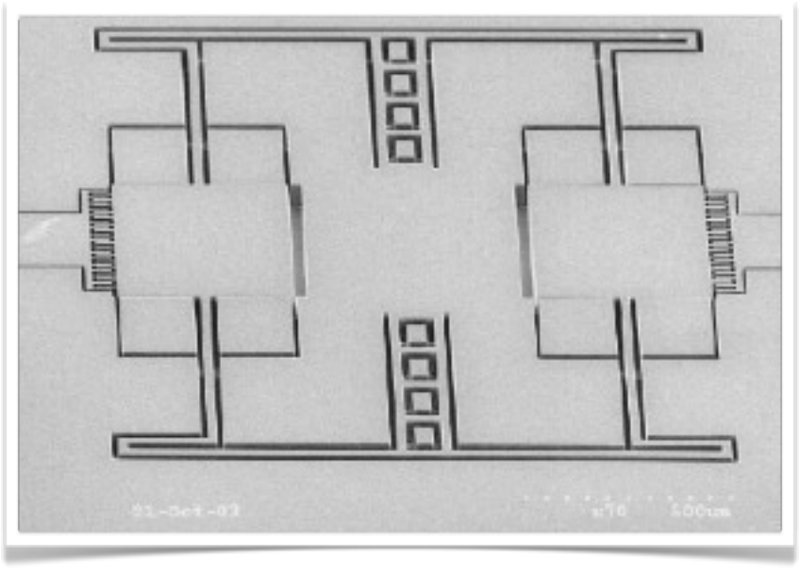
Modeled

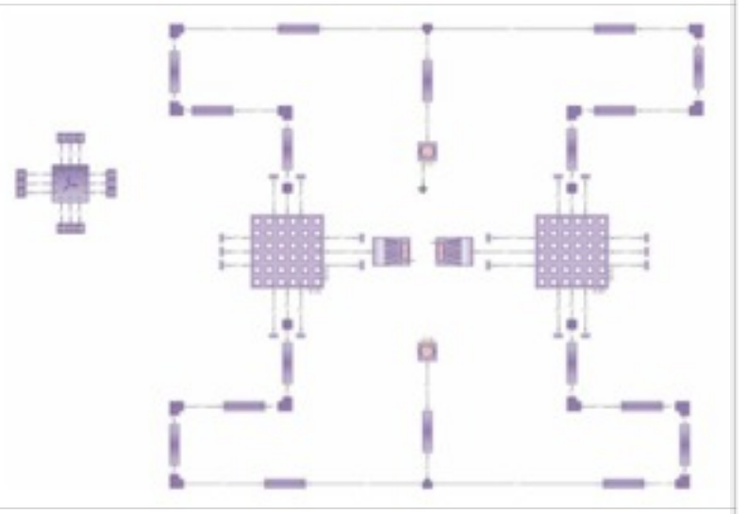


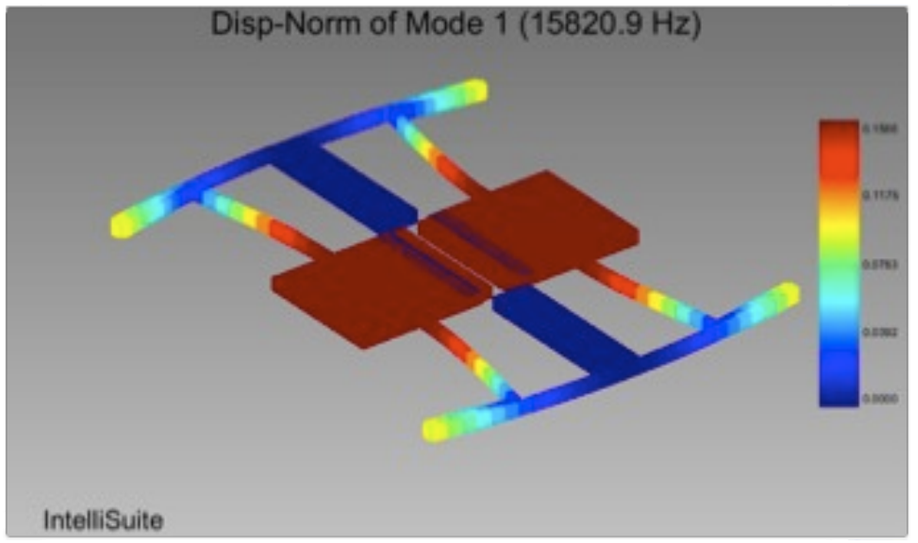

Measured

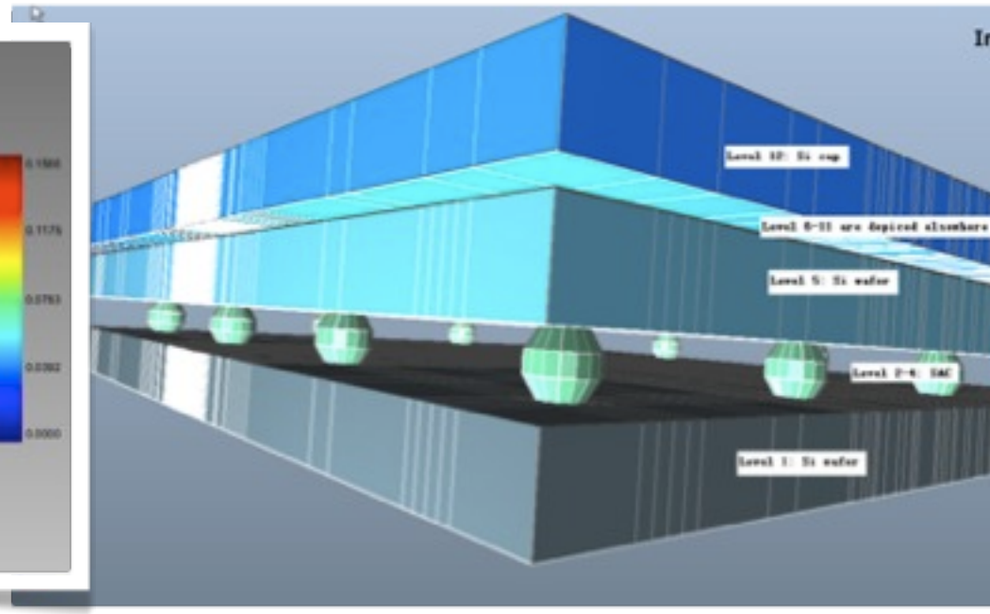


# Mode Matched Tuning Fork Gyro ($M^2$-TFG)





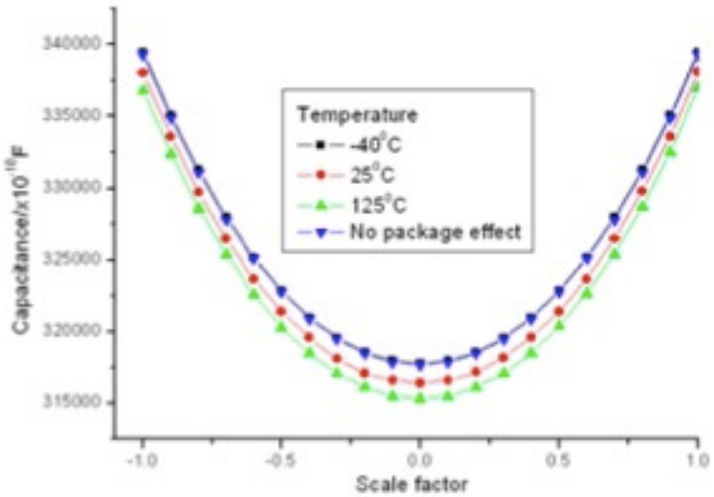


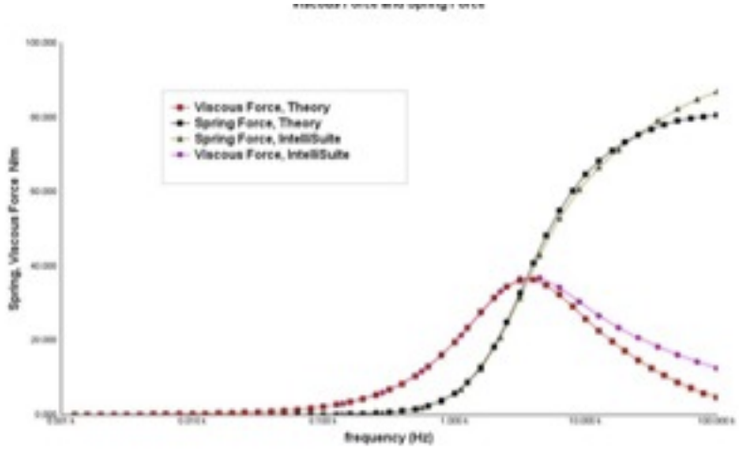



# Mode Matched Tuning Fork Gyro (M²-TFG)

Table 2 Strain energy (×1e-12 J) vs. scale factor of mode 1

| Scale factor | -40℃ | 25℃ | 125℃ | No packaging effects |
|---|---|---|---|---|
| -1 | 51544.9 | 32544.9 | 12941.8 | 47.9935 |
| -0.9 | 51535.7 | 32535.7 | 12932.8 | 38.7439 |
| -0.8 | 51527.5 | 32527.5 | 12924.9 | 30.52 |
| -0.7 | 51520.3 | 32520.3 | 12917.9 | 23.3043 |
| -0.6 | 51514.1 | 32514.1 | 12911.9 | 17.0817 |
| -0.5 | 51508.9 | 32508.9 | 12906.8 | 11.839 |
| -0.4 | 51504.6 | 32504.6 | 12902.7 | 7.5647 |
| -0.3 | 51501.3 | 32501.3 | 12899.5 | 4.24984 |
| -0.2 | 51498.9 | 32498.9 | 12897.2 | 1.88715 |
| -0.1 | 51497.5 | 32497.5 | 12895.8 | 0.471517 |
| 0 | 51497 | 32497 | 12895.4 | 5.22E-07 |
| 0.1 | 51497.5 | 32497.5 | 12895.8 | 0.471503 |
| 0.2 | 51498.9 | 32498.9 | 12897.2 | 1.88711 |
| 0.3 | 51501.3 | 32501.3 | 12899.5 | 4.24983 |




**Strain Energy (Look Up Table)**

**Electrostatic energy**

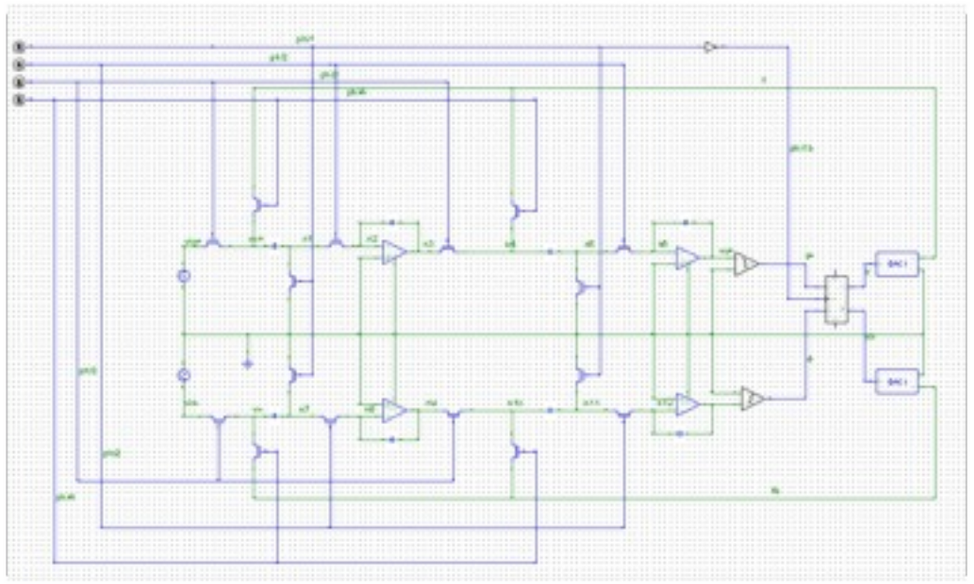
**Fluid damping characteristics**

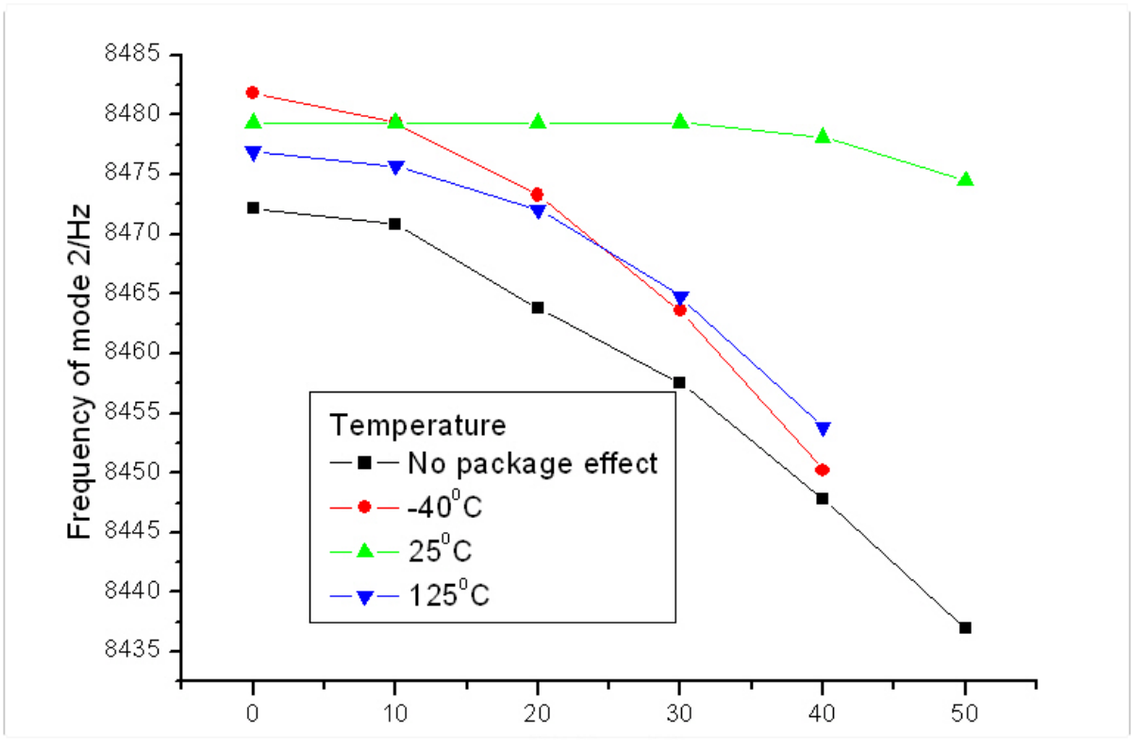
**HDL Model**

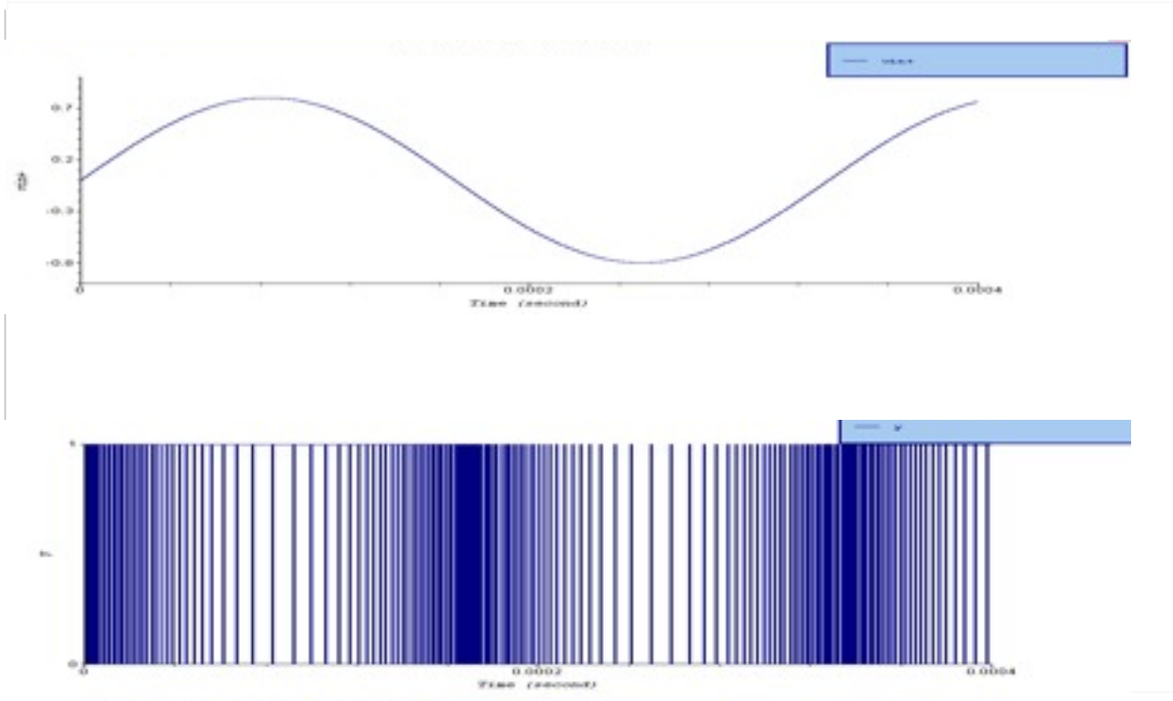
**Cadence, Synopsys, Mentor, Mathworks**

**(Spectre, HSPICE, Eldo, Simulink, System Vision…)**

# Verilog-A modeling results…





# Summary

- New packaging approaches represent an opportunity to rethink MEMS platforms
- MEMS increasingly is subsuming the package
- MEMS Design Is a collaboration challenge
- New generation EDA tools aimed at breaking ‘chain of pain’
  - Allow seamless integration of WLP MEMS+ASIC