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Realizing Area efficient Silicon Micro Structures Using Only Front End Bulk Micromachining

Radharamana Mohanty[1] · **Chanda Karthik**[1] · **Siva Rama Krishna Vanjari**[1] · **Shiv Govind Singh**[1]

Abstract Front-end bulk micro machining is one of the proven techniques of making suspended microstructures and is highly adapted due to its simple and cost effective way of fabricating the devices. In this paper we propose novel geometric mask designs for achieving area efficient microstructures by front-end Silicon (Si) bulk micromachining. In this work we adapt the geometric mask design having a microstructure between two rectangular openings. These openings are aligned at 45° to wafer prime flat of (100) silicon wafer and act as etch openings for front-end bulk micromachining. However rectangular openings lead to high silicon area consumption which makes the process unworthy. Therefore we proposed different geometries to minimize area consumption for achieving the same dimension of suspended structure. All these different geometries are simulated using Intellisuite FABSIM based physical simulator. We have observed more than 28 % reduction in foot print over recent literature and 80 % over the basic design used in this paper.

Keywords Cantilever · Microbridges · Sensors · Si bulk micromachining · MEMS

✉ Radharamana Mohanty
ee11m11@iith.ac.in

Chanda Karthik
ee13m1011@iith.ac.in

Siva Rama Krishna Vanjari
svanjari@iith.ac.in

Shiv Govind Singh
sgsingh@iith.ac.in

[1] Department of Electrical Engineering, Indian Institute of Technology, Hyderabad, Andhra Pradesh, India

1 Introduction

Micro-electro-mechanical systems (MEMS) consist of mechanical components as well as electronic circuits integrated with each other as a complete system. Microfabrication plays a very important role in miniaturizing the mechanical components as a result of which those devices are capable of getting integrated with electronics which as a whole system can be implemented in chip giving very good performance. Surface and bulk micromachining are the two most important processes to make mechanical components [1]. Being simple and cost effective way of removing parts of Silicon, anisotropic wet etching is highly demanded in MEMS processes to make different types of sensors and actuators.

Microcantilevers and microbridges are the frequently used structures in many of MEMS devices. Many of these simple structures are also used as thermal, mechanical and bimolecular detectors. So the ease and cost of process is highly dependent on the fabrication of those microstructures. Using a sacrificial layer of making the device causes difficulty in fabrication while using a SOI wafer makes the cost of the process high. In this paper we propose an efficient way of making Si microstructures using front-end bulk micromachining.

Alignment of the mask patterns relative to wafer crystallographic orientation plays a vital role in fabricating many of the MEMS devices. Because etch rate of anisotropic wet etchant varies depending on the crystal planes get exposed. Etch rate is lower on more densely packed surface than that of loosely packed surface. The structure and dimension of the pattern etched on Si substrate depends not only on the orientation of Si substrate but also on geometry of patterns, its alignment relative to wafer's crystal axes and the duration of etching [2]. In Si (100)

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wafer if the mask(openings) get aligned to ⟨110⟩ direction, i.e., along the wafer flat, then the etched pattern obtained will be bounded by four ⟨111⟩ planes and all those four planes will make an angle of 54.7° with respect to the surface and the etching will eventually stop when all the ⟨111⟩ planes touch. But if the patterns(openings) are aligned at 45° with respect to the wafer prime flat, then all the exposed planes will be ⟨100⟩ in nature, which leads to equal etching in all the directions(both horizontal as well as vertical). Figure 1 shows the etching in (100) wafer where mask oriented in ⟨100⟩ direction. Fang has reported making of Si bridges using bulk micromachining [3] but did not focus on increasing the efficiency of those micro bridges. Here in this paper we propose the efficient mask designs, simulated, fabricated and concluded the most efficient design for making Si micro bridges or the cantilevers.

2 Detailed description

Making mask oriented along ⟨100⟩ direction was a key task to achieve this process. So to achieve this we used one simple but useful technique, where, while making the mask by using mask maker software, we created a line at the bottom of the mask and made all the openings on the mask 45° with respect to it as shown in Fig. 2. During lithography step before exposure we made the line on mask and the wafer prime flat exactly align to each other which was fairly easy task. So now the openings created, are all 45° and hence along ⟨100⟩ direction in the Si wafer. Then for the proof of concept we made the mask with all the above requirements and carried out the experiment to see the etched profile obtained in Si (100) wafer. We made the mask opening at a distance of 200 μm as shown in Fig. 2 and then carried out etching in TMAH for certain time. Then after the etching has done we took the sample and measure the etch depths along lateral as well as vertical direction by using optical profilometer. Figure 4 Shows the Si pillar obtained and Fig. 5, 6 shows the plot of height versus width of the etched pillar obtained.

From the above experiment:

Si width before etching, d = 200 μm.

Pillar width after etching, d − 2x = 134 μm. (x = etch in lateral direction) from Fig. 6.

x = 33 μm and vertical etch, h = 33.2 μm. (From Fig. 6).

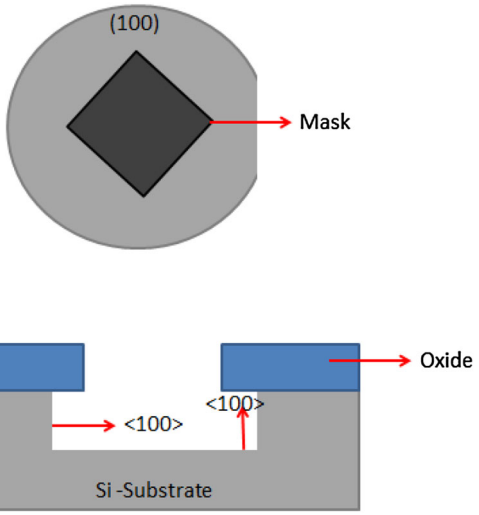
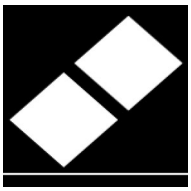


Fig. 1 Etched pattern obtained in (100) Si wafer with mask aligned in ⟨100⟩ direction

Fig. 2 Mask design employed for the fabrication of Si pillar and microbridges



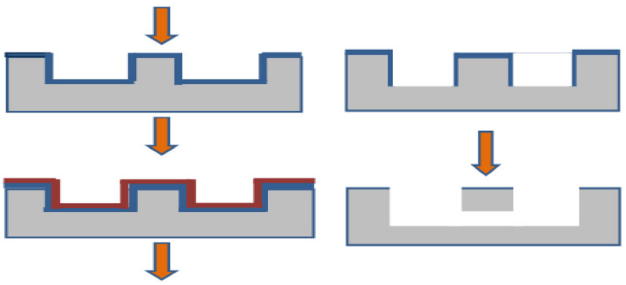


Fig. 3 The steps involved in fabricating Si microbridge

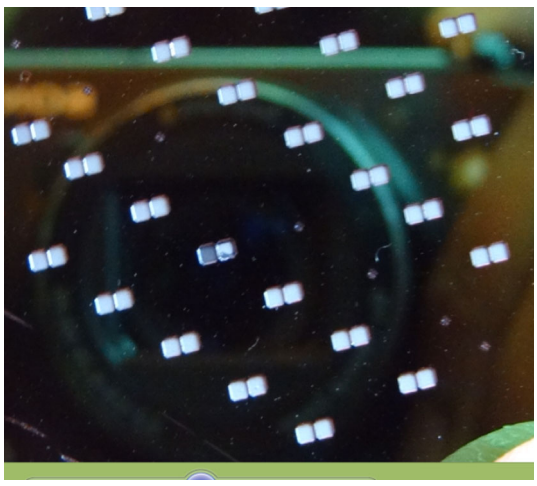


Fig. 4 Etched patterns (Si pillars) obtained in (100) Si wafer with mask aligned in ⟨100⟩ direction

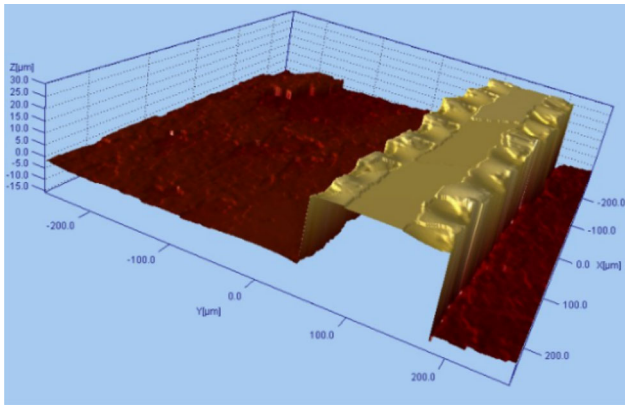


Fig. 5 The optical profilometer image of the etched pattern obtained where mask is in ⟨100⟩ direction

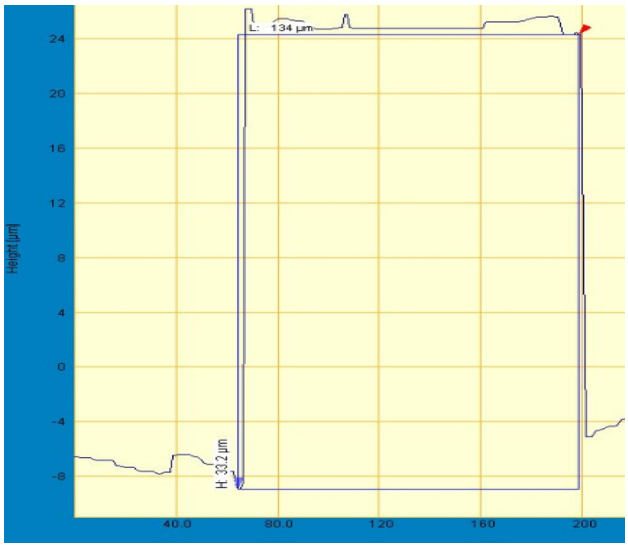


Fig. 6 Height and width of the etched pillar after first etching step

So ratio of lateral etch to vertical etch = x/h = 0.994 ∼ 1.

From the above experiment it was clear that the etched profile we got is vertical in nature instead of inclined plane at 54.7° and the etching, is equal in both the direction, which suggested that all the planes got exposed are same (⟨100⟩) in nature. So from the experiment we thought, if we can control the etch time or the etch depth we can have Si micro bridges and/or cantilevers only in two simple etching steps.

Figure 3. shows the process flow that we adopted to achieve Si microbridge. We carried out several experiments, where in one of the standard experiment, we made the mask where the distance between two openings were 50 µm. In the 1st etching step we etched up to a depth of 15 µm then we oxidized it to protect the sidewalls of Si

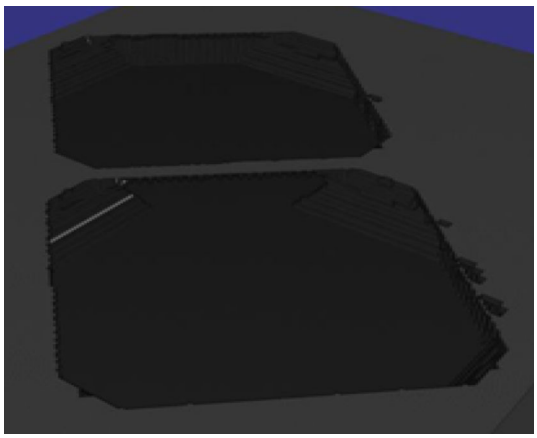


Fig. 7 FABSIM based physical simulation for making Si microbridge

pillar from TMAH and again using the same mask we created the opening on the etched pattern. Now in the 2nd etch step we have done etching up to a depth of approximately 25–27 µm (in total 40–42 µm) which completely released the structure as shown in Fig. 7.

3 Mask designs, simulations and fabrication

The above mentioned process was followed and realized, microbridges with different mask patterns. Figure 8a shows the mask used to create the Si micro bridge, where there are two rectangular openings. Those openings expose all the planes which are ⟨100⟩ in nature but out of all the ⟨100⟩ planes only one ⟨100⟩ plane is useful for making the bridge. All other exposed ⟨100⟩ planes contributed to unnecessary etching outside the concerned area, which increases foot print of each micro bridges. So to reduce the area consumed per device, the mask used in previous case is reduced to half a size as shown in Fig. 8b. Now the mask will expose only two ⟨100⟩ planes and one ⟨111⟩ plane which reduces the area consumed per pixel of Si bridge by more than 50 % as compared to the previous case. Once again the area utilized per device can be reduced with the mask shown in Fig. 8c. Here we reduced the openings for etchant to enter. But it is clear from Fig. 8c that even this opening is more for the required structure. These areas can be saved if we cut half the portion of the mask as shown in Fig. 8d. This mask has advantage over other masks because of having only one opening along ⟨100⟩ plane in the direction where the device is present. So, we designed and optimized our mask in such a way that the etchant will enter and etch in a particular direction i.e. the etching will be directed and is along the direction of concern. This design is one of the most area efficient designs to make the Si micro bridges.

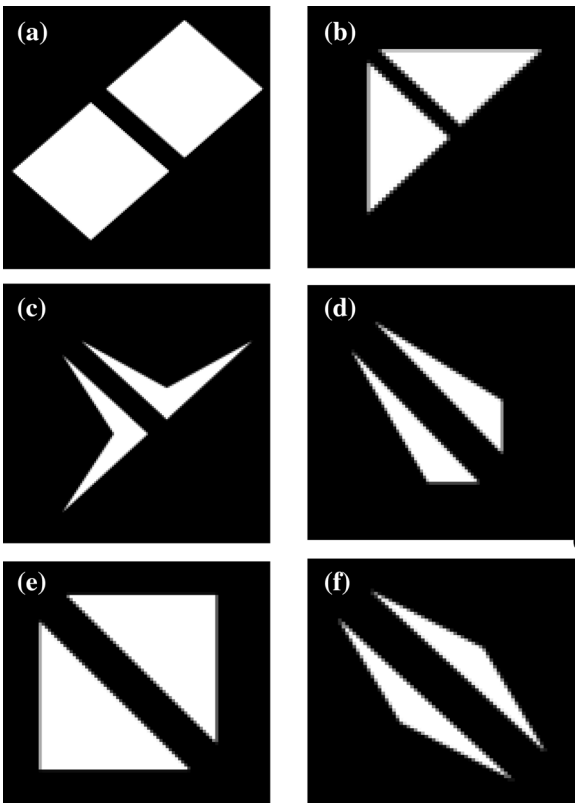


Fig. 8 **a** The mask design-1, making the basic Si bridge. **b** mask design-2, reduces outside etching to one by exposing only one ⟨100⟩ plane outside. **c** Mask design-3, reduced opening leads to save area consumed per Si Bridge. **d** Mask design-4, Minimized area usage for making the Si Bridge. **e** Mask design-5, Secondary method of reducing area utilization per pixel. **f** Mask design-6, for minimized area utilization for secondary method

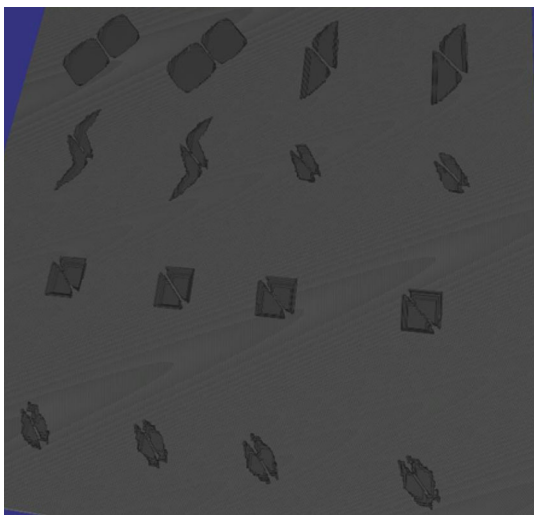


Fig. 9 FABSIM based physical simulation of all the proposed mask designs, showing effectively a comparision of area consumed

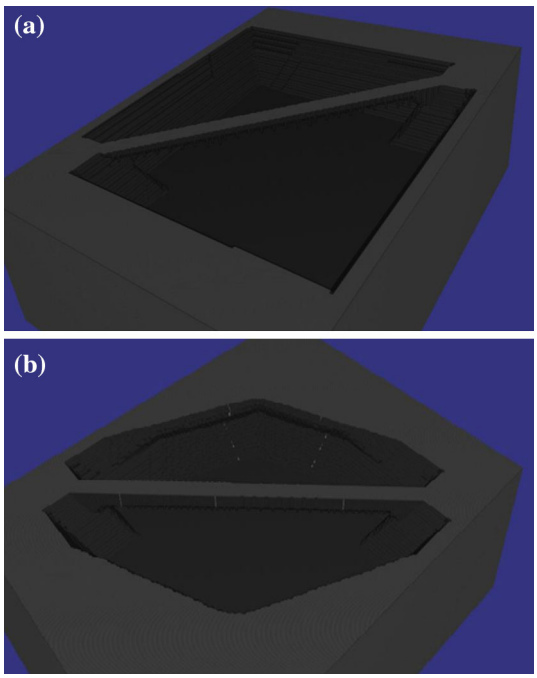


Fig. 10 **a** Single pixel comparison of Si micro bridge using mask design-5, **b** using design-6

Fig. 11 Mask designs designs-7, for four Si cantilever

Another approach to minimize the area consumption per pixel is also presented. Now each triangular opening shown in Fig. 8b is halved so that it will expose only one ⟨100⟩ plane and two ⟨111⟩ planes as shown in Fig. 8e. As a result of which outside etching is prevented to happen because of ⟨111⟩ plane and there will be only inside etching due to ⟨100⟩ plane. Now for further reduction of area per pixel, mask in Fig. 8f is adopted. FABSIM based physical simulations were carried out by considering all the mentioned mask designs which is shown in Fig. 9. Each of the mask designs results in same dimension Si microbridges but varies significantly in area consumed/foot print which is

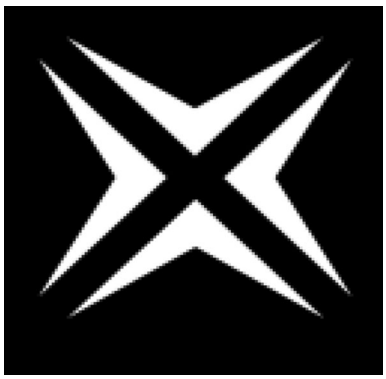


Fig. 12 Mask design-8, area optimized mask for four cantilever beams

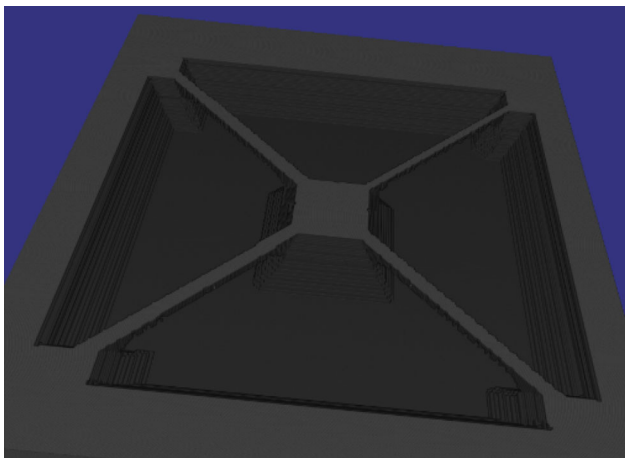


Fig. 13 Intellisuit FABSIM based physical simulation showing the Si bridges

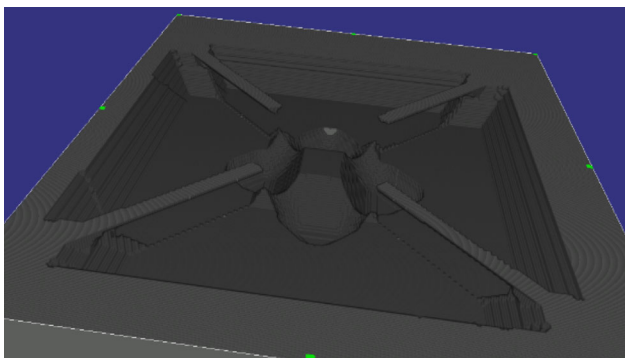


Fig. 14 Intellisuit FABSIM based physical simulation showing cantilever beams

evident from Fig. 9. Once again we put single pixel micro bridge simulation for secondary method using mask design-5 and design-6 in Fig. 10 for a fair comparison of the area consumption.

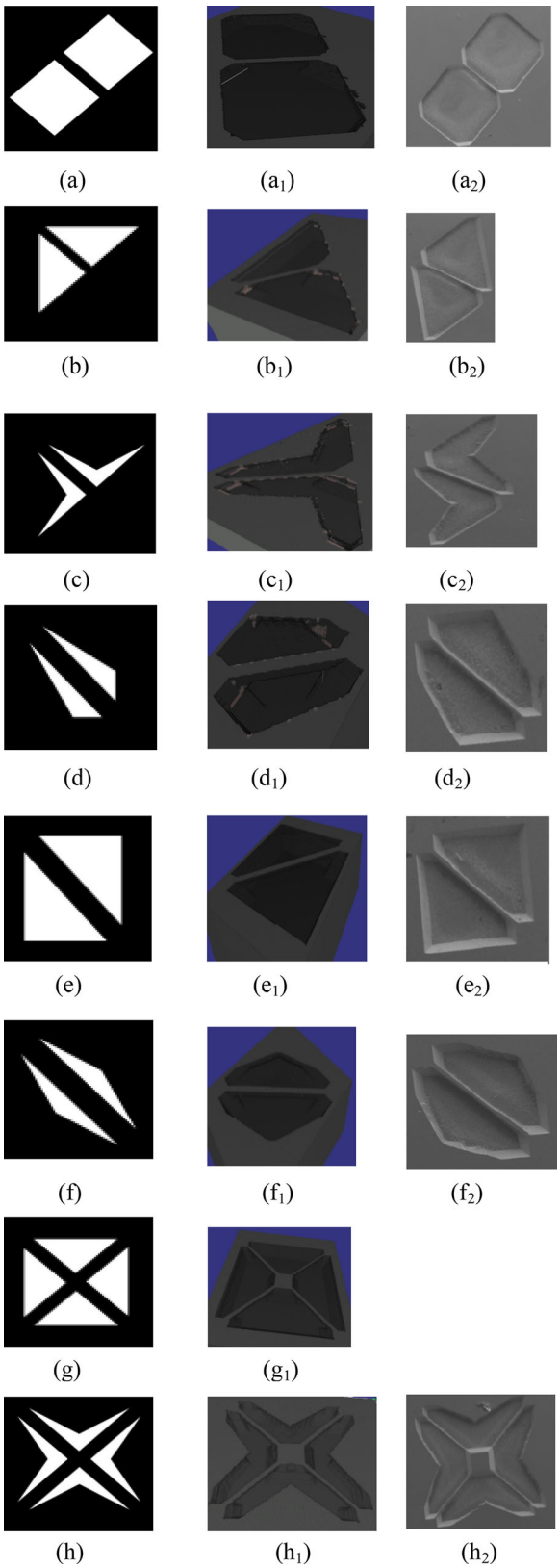


Fig. 15 **a–h** Different mask geometries, $\mathbf{a_1}$–$\mathbf{h_1}$ FABSIM simulation and $\mathbf{a_2}$–$\mathbf{h_2}$ shows corresponding SEM images

4 Enhancement of pixel form factor

This is one of the alternative ideas of making Si microbridges/cantilevers. The mask design-2 (Fig. 8b) will give two directions of freedom for TMAH to etch outside of the concerned direction. If two such structures are kept next to each other, as shown in the Fig. 11 and carryout the same etching processes, it will form four microbridges. Hence if two similar masks of design-2 are used separately then it will result in 2 Si microbridges. But instead of that if we are going for mask design-7 (Fig. 11), we will get 4 Si microbridges. Apart from that the area consumed here will be less because there will be no degrees of freedom for TMAH to etch outside. So this is one of the highly efficient methods of obtaining Si micro bridges in terms of both numbers of devices as well as utilization of area. Further reduction in area can be obtained by the mask design as shown in Fig. 12. We used Intellisuit FABSIM based physical simulation for the mask design-7 and generated the Si microbridges as shown in Fig. 13. Using one more etch step, the central Si Island is etched which results in formation of four cantilever beams as shown in Fig. 14.

5 Results and observations

All the designs mentioned in the paper are listed together and a comparison is done. In Fig. 15a_1–f_1 shows corresponding FABSIM simulation results and the SEM images for each design. Simulated results clearly give the evidence that mask deign-6 is most area efficient. Table 1 shows comparison of area consumption in all the designs in making a Si microbridge. We observed that design-6 has approximately 80 % area saving when compared to basic design (design-1) in this paper and about 28 % when compared to literature [3]. Additionally we design and simulated four leg microbridge and four cantilevers by front end bulk micromachining by using the above mention concepts. Design-8 can be seen as optimum design in terms of area consumed per microbridge. This finding will be useful to fabricate cost and area effective MEMS structure in Si used in various sensors applications. All the above designs have been fabricated and SEM images are shown in Fig. 15a_2–f_2.

The proposed method of making microbridges is very much useful in making micro and nano structures. But if the dimension of the beam required increases and is above micron level then it is difficult to achieve the structures, because large features will require large etch depths which consumes the wafer thickness and wafer thickness is constant for a typical wafer. For example for a 4 inch wafer where the thickness is typically 525 μm, we cannot go beyond an etch depth of 500 μm which limits the beam thickness and width for larger dimensions. But Independent of beam width, the profile that we achieved beneath the beam is always flat and not inclined. This is possible as the planes exposed during etching of silicon are all ⟨100⟩ in nature, similar to the profile that was achieved in the first step, a flat and straight profile is achieved even beneath the beam giving a constant thickness across the width.

We used SiO_2 as a masking layer during etching because growing oxide is simpler and cost effective as compared to any other masking layer. Also the removal of SiO_2 is pretty easy. Hence the process followed above will be a simpler and cost effective method of fabricating Si microbridges.

6 Conclusion

The proposed method of making Si Micro bridges or cantilevers is simple wet etching technique i.e. only using the front-end bulk micromachining reducing the requirement of clean room and also using a single mask thereby reducing the cost. Thus fabricated cantilevers can have wide range of applications with good reliability. Also the

Table 1 The comparison of all the designs presented

Design	Opening area	Exposed ⟨100⟩ planes	Number of beam generated	Area consumption theoretical	Obtained area consumption/μm^2	Area efficiency
Design-1	A[#]	6	1	A + 6σ[$]	111,950	Poor
Design-2	A/2	2	1	A/2 + 2σ	46,326	Average
Design-3	A/2-2X*	2	1	A/2-2X + 2σ	37,953	Good
Design-4	A/4-X	0	1	A/4-X	25,486	Very good
Design-5	A/4	0	1	A/4	31,708	Good
Design-6	A/4-X	0	1	A/4-X	22,823	Very good
Design-7	A	0	4	A	29,161	High
Design-8	A-4X	0	4	A-4X	22,141	Excellent

[#] Opening area per mask, * (X = saved area per opening), [$] etch in ⟨100⟩ plane

efficient mask deigns proposed decreases the foot print of individual pixels and hence increases overall efficiency of the device which may be simple Si micro bridge or complicated structure or even an array where dense structures can be fabricated next to each other.

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