Automatic Generation of a 3-D Solid Model of a Microfabricated Structure

Robert M. Harris, Fariborz Maseeh, and Stephen D. Senturia
Microsytems Technology Laboratories,
Massachusetts Institute of Technology,
Cambridge, MA, USA 02139

1 Introduction

As microfabricated sensors and actuators become increasingly sophisticated and complex, there is an increasing need for CAD tools to permit rational design of these devices. Most critically needed are CAD tools for simulating the mechanical behavior of a sensor or actuator. Simulation presents two fundamental problems[1, 2]: (A) construction of a three-dimensional solid model from a description of the mask layout and process sequence to be used in fabricating the device; and (B) prediction of the material properties of each of the constituent components in the device, including possible process dependence of these properties. We recently presented an architecture that coherently addresses these issues[3]. (See Fig. 1.) In this architecture problem (A) is addressed by a solid modeling tool (the "Structure Simulator") and problem (B) is addressed by a "Material Property Simulator".

Also as part of that work[3], we presented the construction of a 2-D (axisymmetric) solid model for a process sequence of unmasked thermal oxidation optionally followed by removal of the back oxide. This structure was then analyzed using FEM to find the stress distribution in the structure, and, for the single-sided oxide structure, the wafer curvature. Here, we present the automatic construction of a 3-D solid model from a simple process sequence and mask layout along with the simulation and analysis of a simple example. Koppelman[4] has developed a program ("OYSTER") which permits construction of a 3-D polyhedral-based solid model from a mask layout and primitive process description. The differences between Koppelman's approach and the one taken here are discussed in Section 3.

We first give an overview of our CAD system, then the Structure Simulator is described in some detail. Finally, we present the use of the Structure Simulator to simulate wafer bending due to a simple process sequence with a single mask.

2 CAD Architecture

The architecture of our CAD system is shown in Fig. 1. It consists of three basic subsystems (outlined by dashed lines in the figure): Microelectronic CAD, Material Property Simulator, and Mechanical CAD. The interactions among the subsystems and their various components are shown by arrows whose direction specify the direction of information transfer. The "User Interfaces" denote direct user access to architecture components.

This architecture is part of a lager Computer Aided Fabrication (CAF) project which is intended to integrated all phases of design and manufacture of microfabricated devices. Central to this integration effort is a uniform process description, the Process Flow Representation (PFR), to be used for both design and manufacturing[5]. This uniform description allows the designer to simulate the process from the *same* process description that would be used to actually fabricate the device.

The primary interface for mechanical modeling is through PATRAN[6], a mechanical CAD package which provides interactive construction of 3-D solid models, graphical display, and interfaces to FEM packages (we are using ABAQUS[7]). The 3-D geometry resides in the PATRAN Neutral File with additional model information stored separately. We have used the material-property format of the Neutral File in our initial version of the Material Property Simulator.

All of the commercially available code in Fig. 1 is installed and operating. The Structure Simulator has been implemented at an elementary level, and interfaced with the Mechanical CAD subsystem.

In the Microelectronic CAD subsystem, mask layout is created in CIF[8] format using KIC[9], and the process sequence is created in the PFR using a standard file editor. SUPREM-III[10] and SAMPLE[11, 12] are installed to provide depth and cross-sectional process simulation capability. The critical component of this subsystem is the Structure Simulator, which must merge the mask layout and process information to construct a three-dimensional solid model. Two kinds of information must be tracked, the *geometry* of the structure (position, shape, and connectivity of each component), and the *material type* and associated process conditions used to create each component of the structure. The geometry is passed directly to the Mechanical CAD subsection using the PATRAN Neutral File format. The material type and associated process conditions for each component are passed to the interface portion of the Material Property Simulator through what we call the Process History File. A more detailed description of the Structure Simulator is given in the next section.

The Material Property Simulator reads the process sequence for each component of the solid model from the Process History File and generates a set of material property data. The material properties are passed to the Mechanical CAD subsystem, either via the PATRAN Neutral File, the PATRAN interactive (graphics), or directly into the FEM input file. The direct FEM input allows use of an FEM simulator independent of PATRAN;

CH2783-9/90/0000-0036$01.00©1990 IEEE

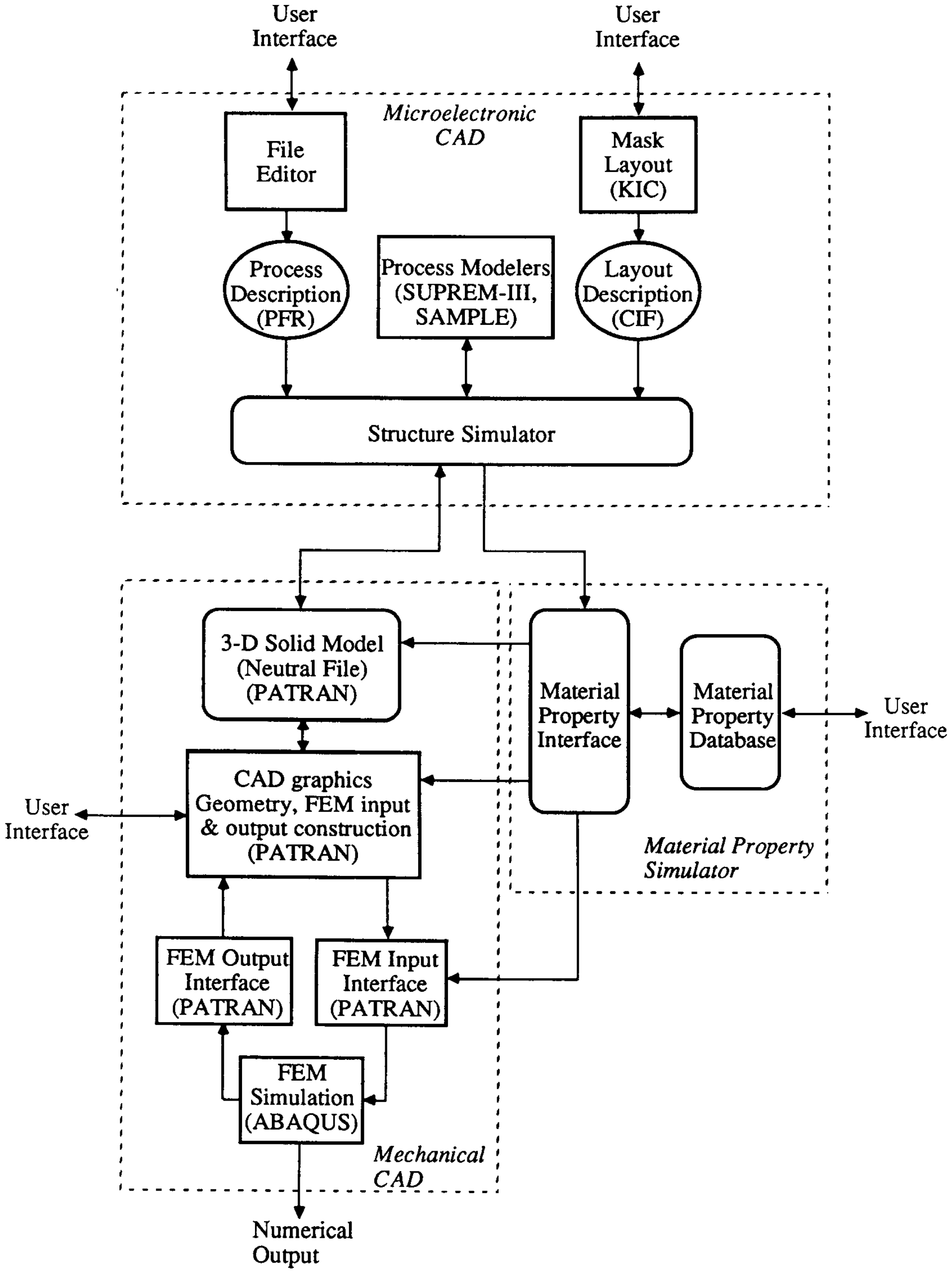
User Interface
User Interface
Microelectronic CAD
File Editor
Mask Layout (KIC)
Process Description (PFR)
Process Modelers (SUPREM-III, SAMPLE)
Layout Description (CIF)
Structure Simulator
3-D Solid Model (Neutral File) (PATRAN)
Material Property Interface
Material Property Database
User Interface
User Interface
CAD graphics Geometry, FEM input & output construction (PATRAN)
Material Property Simulator
FEM Output Interface (PATRAN)
FEM Input Interface (PATRAN)
FEM Simulation (ABAQUS)
Mechanical CAD
Numerical Output

Figure 1: CAD architecture for microelectromechanical design. Arrows denote information flow.

furthermore, it provides for a way to introduce *intrinsic stress* into the mechanical model. (Because of the detailed organization of PATRAN, intrinsic stress must be treated differently than *thermal mismatch stress.*)

Initially, we have elected to use pre-constructed PATRAN-readable data files to manually enter material property data for each type of material which might be a constituent layer of the device. For our example, only data for silicon and silicon dioxide are needed. This method, however, is impractical in the general case, since it requires manual construction of a data set for each possible permutation of material and process conditions. To address this problem, a more sophisticated object-oriented material property simulator is under development and has been described elsewhere[3].

In the Mechanical CAD subsystem, the geometric information from the Structure Simulator is discretized into finite elements, material properties from the Material Property Simulator are associated with their proper geometries, and the appropriate loads and boundary conditions specified. The solid model geometry and material properties are read and manipulated in PATRAN graphics, and a complete finite element input model is generated and optimized interactively. The FEM model is then translated into an ABAQUS input file for FEM analysis. (Intrinsic stress would also be entered into the input file at this point.) The results of the FEM analysis are then translated back into a PATRAN-readable form for display. PATRAN can then be used to examine simulated mechanical behavior of the device.

3 Structure Simulator

The Structure Simulator works on a process-step-by-process-step basis, modifying the solid model after each process step. This mimics the physical fabrication sequence, in which each process step causes a change in the wafer. The final structure is therefore the result of a sequence of such changes. The step-by-step operation of the Structure Simulator also permits simulation of intermediate results of the process sequence. This can be used, for example, to simulate whether the structure will maintain mechanical integrity throughout the entire process sequence.

For each process step, the Structure Simulator begins by reading the current step from the PFR, and the effect of this step is determined. (For example, the process *step* "oxidize in wet O_2 for 4hrs. at 1000°C" is converted into the process *effect* "grow 1 μm silicon dioxide on bare $\langle 100 \rangle$ silicon".) When necessary, the PFR information is passed to process simulators (e.g., SUPREM-III, SAMPLE) and the simulation results are used to determine the process effect. (In Koppelman's program, OYSTER[4], the process effect is entered directly using its Process Description Language (PDL). OYSTER, therefore, bypasses this step.) Layout information is consulted using the OCT database[13]. Although OCT is a general purpose database for microelectronic design, we use it here solely as a programmatic interface to the CIF layout description.

Modification of the solid model based on the process effect is done in two steps. First, the process effect is decomposed into a combination of primitive construction operators. These primitive operators are then used to modify the solid model from the previous process step, both the geometry (in the Neutral File), and the material-type information (in the Process History File). The updated model is output for use with the next process step. The above sequence is then repeated for the next process step. The operation of the Structure Simulator is summarized in Table 1.

Table 1: Summary of Structure Simulator Operation

1. Determine effect of process step.
   Consult layout information and process modelers, as necessary.
2. Decompose process effect into primitive construction operators.
3. Modify solid model using primitive operators.
4. Output results
   Geometry information ⇒ Neutral File
   Material information ⇒ History File
5. Repeat steps 1–4 for next process step.

Modification of the solid model must be implemented to ensure that the resulting model is physically valid (i.e., describing a reasonable approximation to the actual structure). Without careful attention to the robustness of modification algorithms, invalid solid models could result (e.g. an unphysical topology such as a Klein bottle, or two objects occupying the same place). Implementation of a robust modification algorithm is considerably simplified if the modification is done using a small set of robust primitive construction operators. Hence, the two step modification procedure discussed above. For micromechanical design, the following primitive operators constitute a useful minimal set: film deposition and growth, film etching, impurity introduction and movement, and wafer joining. These primitives are combined using selection operators which restrict the operation of primitive operator to a certain region of the solid model. Selection may be done on the basis of layout (masking) or material type. For initial implementation, we have selected a restricted subset of operators: conformal deposition, and masked etching. These two primitives provide significant geometry flexibility, and permit the simulation of many interesting micromechanical systems.

The Structure Simulator must output the final structure to the Mechanical CAD subsystem for use in mechanical simulation. Therefore, the solid model representation used by Structure Simulator must be compatible with the one used by our Mechanical CAD, in this case PATRAN. Rather than convert from one solid model representation to another, the Structure Simulator uses the same solid model representation as PATRAN, which is analytic solid modeling (ASM). In ASM a solid is represented as an assemblage of non-overlapping hyperpatches[14]. A hyperpatch is essentially a distorted cube and is generated by mapping a unit cube in parametric (ξ_1,ξ_2,ξ_3) space into the model (x,y,z) space using a tricubic function. In general, a hyperpatch is defined by,

$$Z(\xi_1, \xi_2, \xi_3) = \sum_{k=1}^{4} \sum_{j=1}^{4} \sum_{i=1}^{4} S_{ijk} \xi_1^{4-i} \xi_2^{4-j} \xi_3^{4-k} \qquad (1)$$

where Z is a vector in the model space and the $\{S_{ijk}\}$ are arbitrary vector coefficients. The advantages of ASM are that it allows modeling of the solid interior as well as the boundary and, due to the cubic mapping, can model curved surfaces. This is at the cost, however, of increased model complexity. In a boundary representation solid model, a continuous layer can be represented as a single entity with a complicated boundary. In ASM, this layer must be broken up into an assemblage of hyperpatches.

OYSTER[4] functions like our Structure Simulator, in that it combines layout and process information to produce a 3-D solid model. There are two basic differences in design between it and the Structure Simulator presented here. As mentioned above, OYSTER's process description, PDL, describes the process *effects*, not the process *steps* which would be used to actually fabricate the device. Secondly, OYSTER is built upon a polyhedral solid modeler and cannot model curved surfaces directly. Instead, a curved surface must be broken into facets. This could pose later difficulties in mechanical analysis due to artificial stress concentrations at facet corners.

Despite these differences, OYSTER is similar in many ways to the Structure Simulator presented a here. It works on step-by-step basis following procedure similar to that given in Table 1 (except for omitting Step 1 as described above). OYSTER also modifies the solid model using combination of robust primitive operators. In this case, the primitive operations are solid boolean operations (provided by the underlying solid modeler). The are combined into "cumulative translation sweep" operators to do the actual modifications[15].

Because of the current incomplete and elementary implementation of primitive construction operators in our Structure Simulator, OYSTER, at present, has a far superior modeling capability.

4 Example

The specific process considered in this example is: a 4-inch (100) silicon wafer is thermally oxidized at 1030°C in wet ambient for four hours. This grows just over 1 μm of silicon dioxide on both sides of the wafer. The oxide is removed from the back and a rectangular hole is optionally patterned and etched in the front oxide of each 10mm-square chip. The wafer is then diced into individual chips. Due to the compressive residual stress in the oxide layer the chip bends. This bending is less pronounced as larger holes are etched in the oxide.

The Structure Simulator is used to create a solid model of the chip in PATRAN Neutral File format. Currently, the Structure Simulator does not read the process sequence directly from the PFR. Instead, the program queries the user directly for the necessary information. The process history information is maintained manually by the user.

The program begins by asking for information about the starting wafer state (thickness, orientation, and chip dimensions). The program then constructs a linear hyperpatch (see Fig. 2(a)) whose thickness is the wafer thickness and whose length and width is given by the chip dimensions. The oxidation conditions are specified by temperature, time, and ambient. Using this information and the starting wafer state the program constructs a SUPREM-III input file, and runs SUPREM-III to calculate the oxide thickness that would be grown. Two linear hyperpatches of this thickness are attached to the front and back sides of the starting wafer to represent the oxide. The thickness of the starting wafer is also thinned at this time based on the SUPREM-III simulation results. This implements the planar growth operator. The result after this process step is shown in Fig. 2(b). Finally, the masked oxide etch is specified by the OCT cell name and layer to be used. (Complete etching of all unmasked oxide is assumed.) The program queries the OCT database and extracts the mask geometry of the desired layer. Currently, only a single layer with a single rectangular

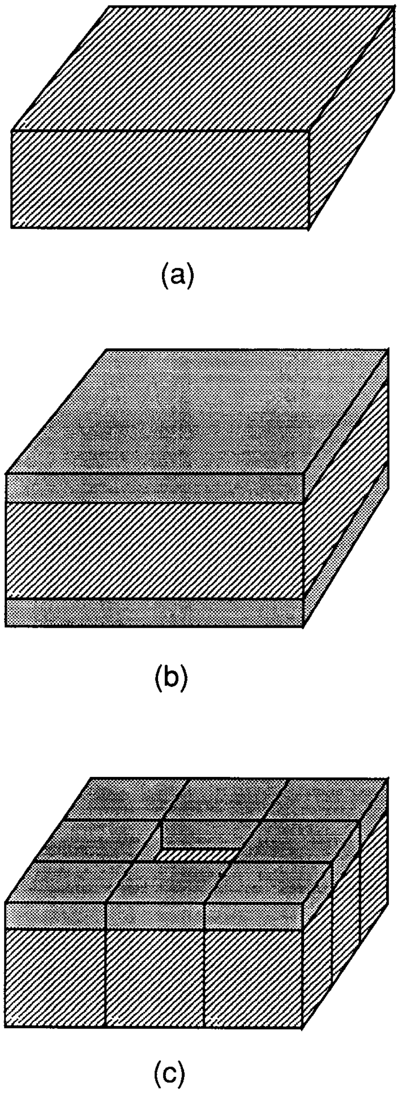

Figure 2: Three-dimensional solid models of the example process.
(a) starting wafer. (b) after application of planar growth operator (oxidation) (c) after application of masked etch operator

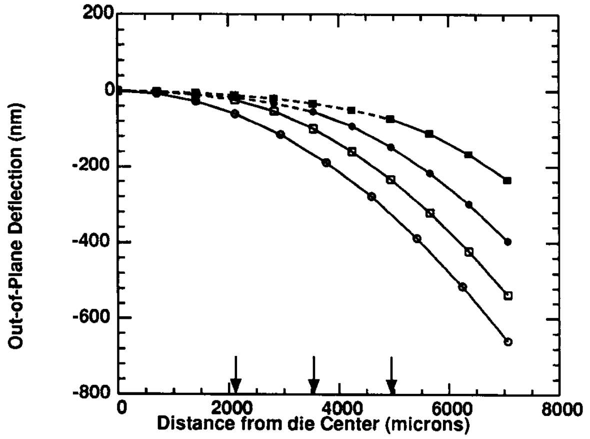

Figure 3: FEM results for intact oxide, 3mm-, 5mm-, 7mm-square holes (o,□,●,■ respectively) along the diagonal from chip center to chip corner. Solid lines (—) are used for the area under the unetched oxide; dashed lines(- -) for the etched oxide. Arrows (↓) show distance from center of oxide hole edges.

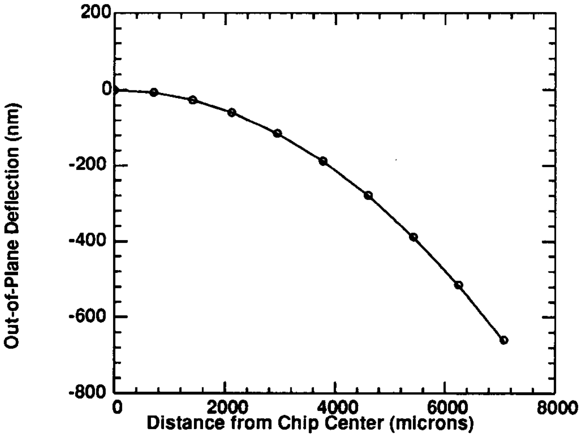

Figure 4: Comparison of Stoney Equation (—) with FEM results (o) for intact oxide

box is supported. To do the etch, the hyperpatch representing the back oxide layer is deleted, and the front oxide hyperpatch is divided into a 3x3 grid. The center hyperpatch of this grid is then deleted, thus implementing a masked removal operator. The final structure is shown in Fig. 2(c). In this example undercutting during the etch has been ignored — the sidewalls are vertical and the corners square. This is sufficient for deformation analysis but not for stress analysis. Curved sidewalls could be included in the solid model by replacing the linear hyperpatches with more elaborate ones.

The resulting structure (stored in PATRAN Neutral File format) is used directly by PATRAN. Using the PATRAN the structure is discretized (800 20-noded elements are used for the silicon and 400 20-sided elements are used for the unetched oxide layer) and appropriate boundary conditions are applied. Material properties are associated with each layer, in this case, by reading from a pre-constructed data file containing information on silicon and silicon dioxide. A thermal cooling load of −1000°C was applied to the entire model, generating a residual stress due to the mismatched coefficients of thermal expansion. *Intrinsic* residual stress was ignored in this analysis.

PATRAN is then used to optimize the FEM model and create an ABAQUS input file. ABAQUS is then run to do the actual analysis. The analysis results are translated into a PATRAN compatible form through an ABAQUS-to-PATRAN translator. PATRAN is then used to graphically display and examine the final results.

Calculated deformations along a diagonal form chip center to chip corner for the unetched oxide layer, and layers with 3mm-, 5mm-, and 7mm-square holes are shown in Fig. 3. As can be seen in the figure, as the hole size increases the amount of deflection decreases. Also, the chip curvature where the top oxide has been removed is markedly shallower than underneath the unetched oxide.

For the case of unetched oxide, film stress is related to out-of-plane bending of the substrate by the Stoney equation[16]:

$$\sigma_f = \frac{4}{3}\frac{E_s}{1-\nu_s}\frac{t_s^2}{t_f}\frac{z}{L^2}, \tag{2}$$

where σ_f, E_s, ν_s are the film stress, substrate Young's modulus, and substrate Poisson's ratio; t_s and t_f are the substrate and film thicknesses; and z and L are the out-of-plane deflection and length over which the deflection is measured. As can be seen in Fig. 4, analytic results given by the Stoney Equation are almost indistinguishable from the simulated deformation of the unetched oxide layer.

It should be noted that as the structure complexity increases, computer resources are rapidly exhausted during the mechanical analysis. For the relatively coarse discretization used here, 7 hrs of CPU time on a Sun-4/200 and 160 MBytes of scratch disk space were required.

5 Conclusion

We have demonstrated the automatic construction of a 3-D solid model from a specification of mask layout and process sequence, the process sequence, the process sequence consisting of planar deposition and masked etch. The generated 3-D solid model is directly usable by our mechanical CAD software and was used to do a deformation analysis of the structure.

Acknowledgments

The authors gratefully acknowledge Duane Boning for providing the code that interfaces with SUPREM-III and for critical review of this manuscript. This work is supported in part by the Department of Justice under contract J-FBI-88-067 and DARPA under contract MDA972-88-K-0008 and is carried out in the Microsytems Technology Laboratories of the Massachusetts Institute of Technology.

References

[1] S. D. Senturia, "Microfabricated structures for the measurement of mechanical properties and adhesion of thin films," in *Transducers '87*, (Tokyo), pp. 11-16, 1987.

[2] S. D. Senturia, "Can we design microrobotic devices without knowing the mechanical properties of materials?," in *IEEE MicroRobotics and Teleoperators Workshop*, (Hyannis, MA), 1987.

[3] F. Maseeh, R. M. Harris, and S. D. Senturia, "A CAD architecture for microelectromechanical systems," in *Proc. IEEE Micro Electro Mechanical Systems*, (Napa Valley, CA), pp. 44–49, 1990.

[4] G. M. Koppelman, "OYSTER, a three-dimensional structural simulator for microelectromechanical design," *Sensors and Actuators*, vol. 20, pp. 179–185, Nov. 1989.

[5] M. B. McIlrath and D. S. Boning, "Integrating semiconductor process design and manufacture using a unified process flow representation," in *Proc. 1990 Intl. Conf. Computer Integrated Manufacturing*, May 1990.

[6] PDA Engineering, Costa Mesa, CA.

[7] Hibbit, Karlsson, and Sorensen, Inc., Providence, R.I.

[8] L. Conway and C. Mead, *Introduction to VLSI Systems*, pp. 115–127. Reading, MA: Addison-Wesley, 1980.

[9] G. C. Billingsley, "Program reference for KIC," Tech. Rep. UCB/ERL M83/62, U. C. Berkeley, Oct. 1983.

[10] C. P. Ho, J. D. Plummer, S. E. Hansen, and R. W. Dutton, "VLSI process modeling SUPREM-III," *IEEE Trans. Electron Dev.*, vol. ED-30, pp. 1438–1452, Nov. 1983.

[11] W. G. Oldham, S. N. Nandgaonkar, A. R. Neureurather, and M. M. O'Toole, "A general simulator for VLSI lithography and etching process: Part I — application to projection lithography," *IEEE Trans. Electron Dev.*, vol. ED-26, pp. 717–722, Apr. 1979.

[12] W. G. Oldham, A. R. Neureurather, C. Sung, J. L. Reynolds, S. N. Nandgaonkar, and M. M. O'Toole, "A general simulator for VLSI lithography and etching process: Part II — application to deposition and etching," *IEEE Trans. Electron Dev.*, vol. ED-27, pp. 1455–1559, Aug. 1980.

[13] D. S. Harrison, P. Moore, R. L. Spickelmeyer, and A. R. Newton, "Data management and graphics editing in the berkeley design environment," in *Technical Digest of ICCAD-86*, (Santa Clara, CA), pp. 20–24, Nov. 1986.

[14] M. S. Casale and E. L. Stanton, "An overview of analytic solid modeling," *IEEE Computer Graphics and Applications*, vol. 5, no. 2, pp. 45–56, 1985.

[15] R. C. Evans, G. Koppelman, and V. T. Rajan, "Shaping geometric objects by cumulative translational sweeps," *IBM J. Res. Dev.*, vol. 31, pp. 347–360, 1987.

[16] G. G. Stoney, "The tension of metallic films deposited by electrolysis," *Proc. R. Soc. London, Ser. A*, vol. 82, p. 172, 1909.