N/MEMS Design Methodologies

Efficient workflow for robust, first-time-right design

White Paper

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Contents

Think big.

Make no little plans. They have no magic to stir men's blood and probably themselves will not be realized. Make big plans; aim high in hope and work, remembering that a noble, logical diagram once recorded will never die, but long after we are gone will be a living thing, asserting itself with ever-growing insistency. Remember that our sons and grandsons are going to do things that would stagger us. Let your watchword be order and your beacon beauty. Think big." — DANIEL BURNHAM, CHICAGO ARCHITECT.(1864-1912)

Executive summary

As N/MEMS devices grow ever more complex and start to reach large-volume markets in consumer electronics, automotive and telecommunications, there is a need for efficient, yet accurate methodologies that can deliver first-time-right design.

While the industry has made significant progress in process technology, the fact remains that every successful MEMS device has a unique process flow. In fact, the industry is moving toward standardized process modules that can be combined into a custom process flow. While the shift to 8" and larger substrates will help in consolidating the number of process flows, successful MEMS design tools should recognize the "*one device, one process*" mantra and help the designer drill down the process options using quantitative methods. Compounding the challenge is the fact that accurate statistical process control (SPC) data is often not available. Designers often estimate the process variations based upon past experience and use these tolerances to guide their design decisions.

As MEMS make their successful entry into mobile devices, the demand for slim profile packages becomes paramount. MEMS devices have started to leverage IC stacking technologies such as wafer bumping, die-on-wafer assembly, through-silicon vias (TSV) and towards low-cost Wafer Level Chip Scale Packages (WLCSP). As the MEMS subsumes the package into the structure, the need for efficient package modeling and compensation of packaging effects at the die level become important.

Time-to-market pressures are driving concurrent design of the micro-mechanisms, package and corresponding electronics. Efficient tools to capture device, package and system level effects become paramount. Linear, iterative design flows quickly become a bottleneck for the MEMS organization.

Fortunately, structured design flows that can efficiently interchange information between the schematics, process flows, layout, 3D FEA/BEA, and package analysis can allow the MEMS organization to exchange information between process, design, electronics, packaging, integration and software engineers. This white paper is intended to illustrate how budget-constrained organizations can implement a friction-free workflow to achieve first-time-right designs.

N/MEMS Design Today

As the N/MEMS industry matures, the design challenge continues to move from the microstructure design to the microsystem design. With the maturity of the process technology and the increase in computing power, designers are now looking to optimize MEMS from a system standpoint. Traditional N/MEMS CAD tools provide functionality to design at a microstructure level.

Today MEMS modeling and simulation is performed at various levels of granularity by MEMS engineers working on different aspects of the manufacture. *Ab initio* models are based upon atomistic, quantum mechanical or molecular dynamics. Such models are typically used in process modeling to predict material behavior (such as physical properties or etch behavior). Component level models can include lumped models and finite element representations of a component such as a plate or a comb drive. Device models represent the working of the micro or nanostructure under investigation. Algorithmic models are used to capture the behavior of a certain logic or control element within a system. Finally, system level models are used to model the entire microsystem.

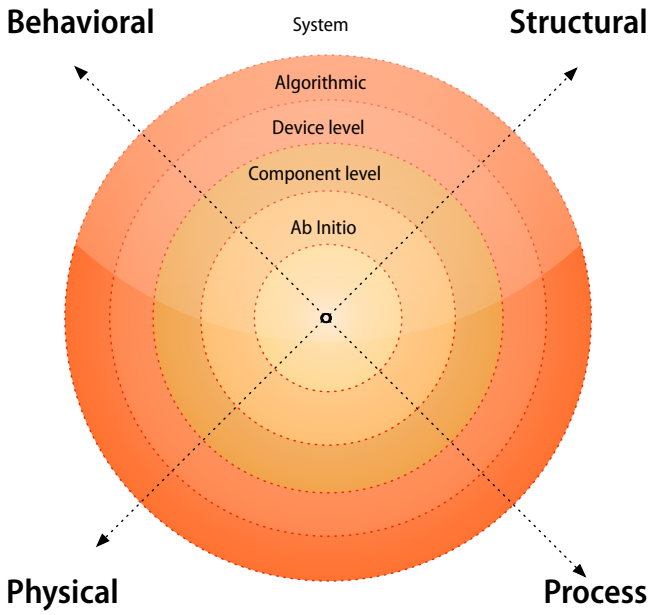


Figure 1: *X-Diagram for Micro and Nano-system development, illustrating various levels of granularity of the design.*

Ab initio (first principles) simulations

First principle simulations are typically based on atomistic or quantum mechanical molecular dynamics principles. These are typically useful in predicting material properties or predicting phenomenon at the nano-scale. While, this is a growing area of research, only a few tools have made it into the everyday repertoire of the MEMS design engineer. One such tool is IntelliSense's IntelliEtch which uses atomistic principles to simulate the etching of silicon.

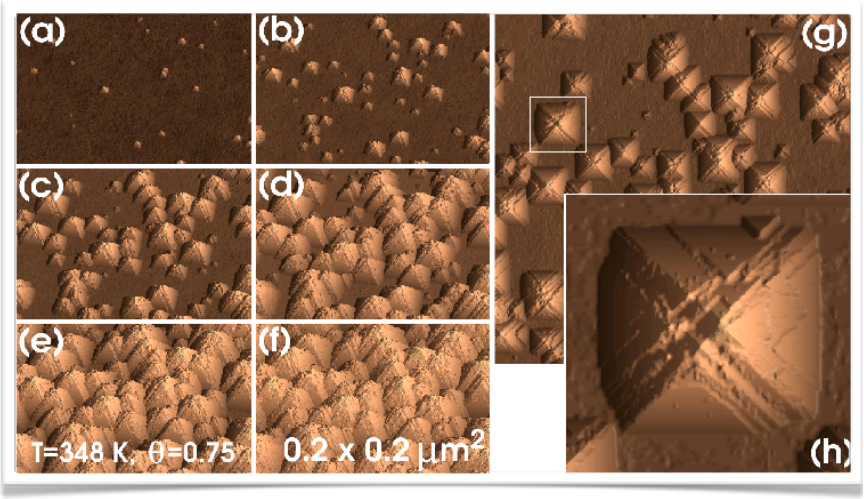
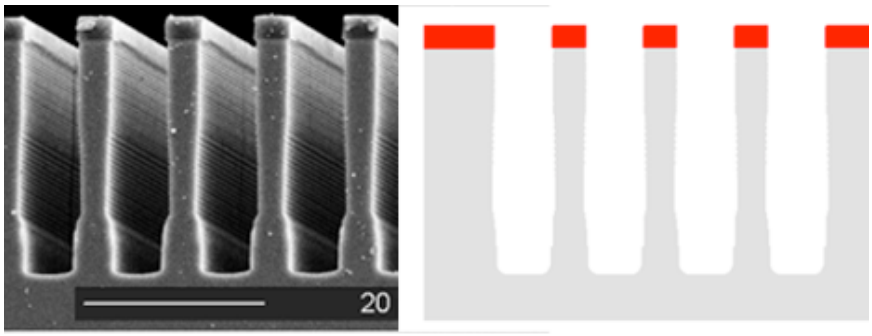


Figure 2: *Atomistic calculations are used to predict hillock formation and surface morphology during wet etching of silicon. Ab initio techniques allow the user to capture effects of micro-masking which can lead to hillock formation, preventing smooth etches.*

Technology CAD (TCAD)

At this level, the microstructure is simulated at the process level. Simulators such as AnisE™ and RECIPE™ from IntelliSense and SUPREM™-based simulators from various vendors simulate the actual process flow based upon process settings and physical simulation of the process, such as diffusion, growth or etching. TCAD-based models are typically set up and run by process engineers.

These simulations are useful in understanding the effect of the process on the final physical geometry of the device. Since they are based on the actual physical models, they are often very time-consuming. For instance, IntelliSense's RIE/ICP simulation tool RECIPE is based on the actual simulation of the plasma etching process and polymer deposition process. These tools are used to determine the influence of the process and mask set on the final geometry of the device.



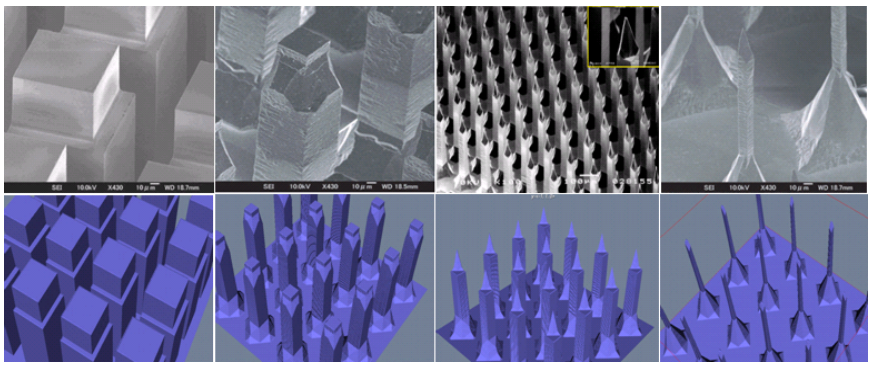


Figure 3 *: Technology CAD (TCAD) tools are used to accurately predict the physical etching and processing of MEMS devices.*

***Above**: comparison between experiment and simulation of Deep Reactive Ion Etching (DRIE) of silicon. Sidewall angle tuning is integral for high performance of many classes of MEMS devices.*

***Below**: A complex process of formation of micro-needles being simulated in software.*

Process flow design (Process CAD)

The bane of every MEMS process engineer is creating and recreating flow diagrams (2D cross sections) of the process flow, while some process engineers still use 2D drawing tools such as Adobe Illustrator or PowerPoint. Increasingly sophisticated tools such as FABViewer and CSViewer (integrated into IntelliSense's Blueprint) have started to address this market. These tools can be used to output process flows directly into Powerpoint or other presentation tools.

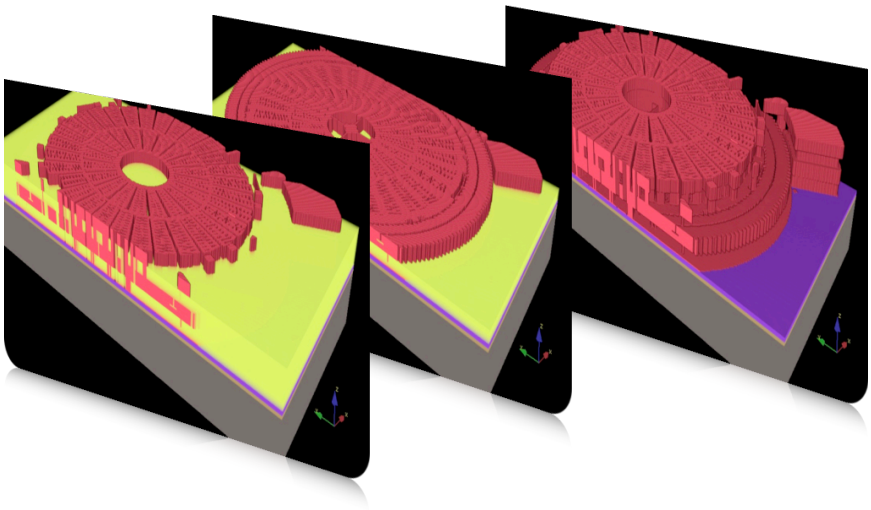


Figure 4 : *Snapshots from the process visualization of a rotary Vibro-drive fabricated using the Sandia Summit-V process. Courtesy: Prof Tim Dallas*

Schematic or component based design (Top-down design)

One of the primary advantages behind a hierarchical approach is that the design entry is done in terms of fundamental building blocks or components. This allows the user to enter a parameterized model of the device in terms of both layout and manufacturing data.

Since the data entry is done in terms of parameterized abstract models, users can analyze the devices at different granularities. The atomic element model can be represented in terms of lumped models, distributed models, or Rayleigh-Ritz based FEA/BEA models. The user can then easily perform an accuracy-time trade-off.

One of the disadvantages of schematic-based design is that the user is limited to using components in the design library. Arbitrary geometries and new physical or material models are difficult to incorporate into the design. Since most schematic models are, to a degree, based on lumped models, they cannot accurately capture second-order effects and non-linearities.

For instance, accurate capture of electrostatics, fluidics or contact and post-contact physics in arbitrary geometries requires full 3D modeling. Similarly, packaging level effects such as influence of viscoelastic overmolds, effects of die bumping and substrate attach are difficult to capture in component-based models.

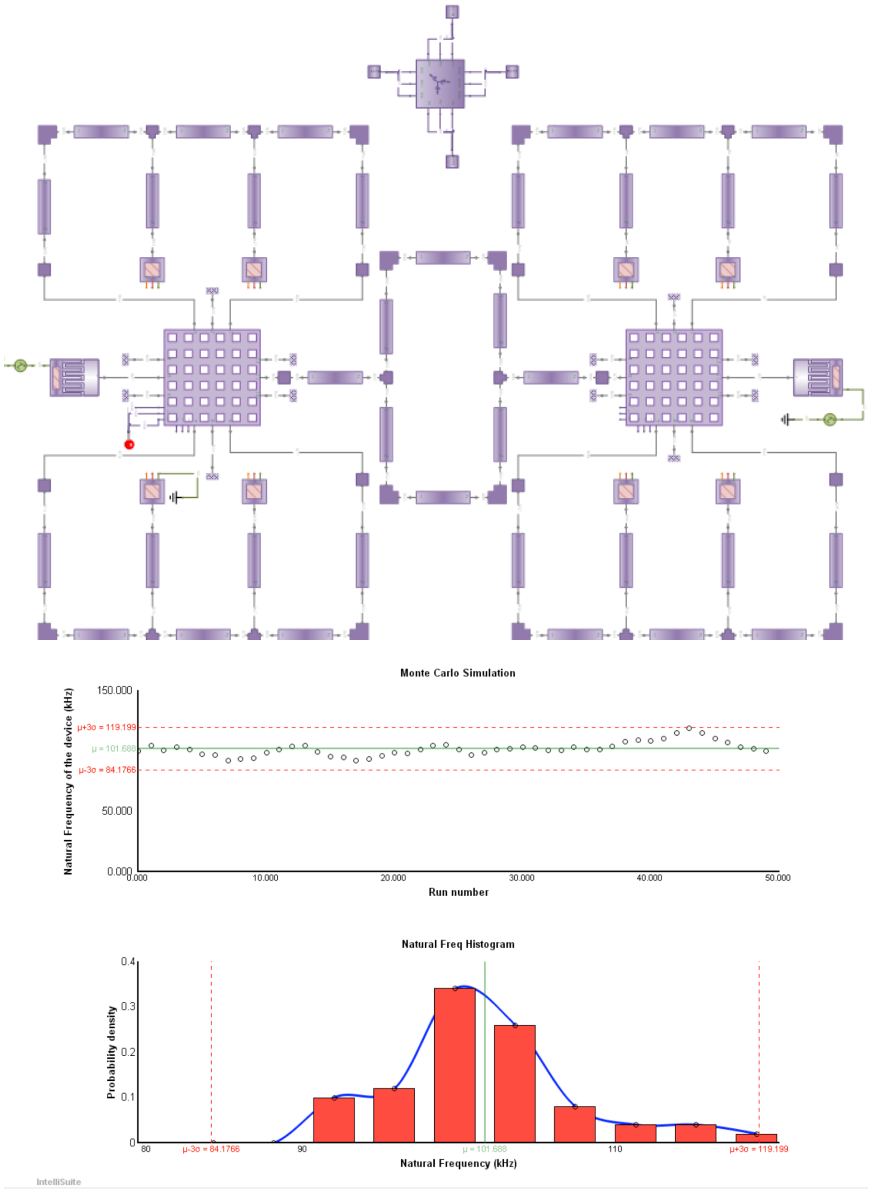


Figure 5 : *Schematic of a bandpass filter in SYNPLE. SYNPLE allows you to quickly setup a parametric model of your MEMS device.*

The figure below shows the results of a Monte Carlo simulation plotting the anticipated variation of natural frequency. Use of compact models allows users to develop robust designs that are inherently manufacturable.

Schematic synthesis

Schematic synthesis tools, such as those incorporated in SYNPLE can convert component-based schematics into ready-to-use mask layouts, or hexahedral meshes that can be further used in 3D analysis of microsystems.

Figure 6 *: MEMS design is inherently multi-domain in nature. The figure depicts the different kind of models that need to be incorporated in the modeling of a vibro-drive.*

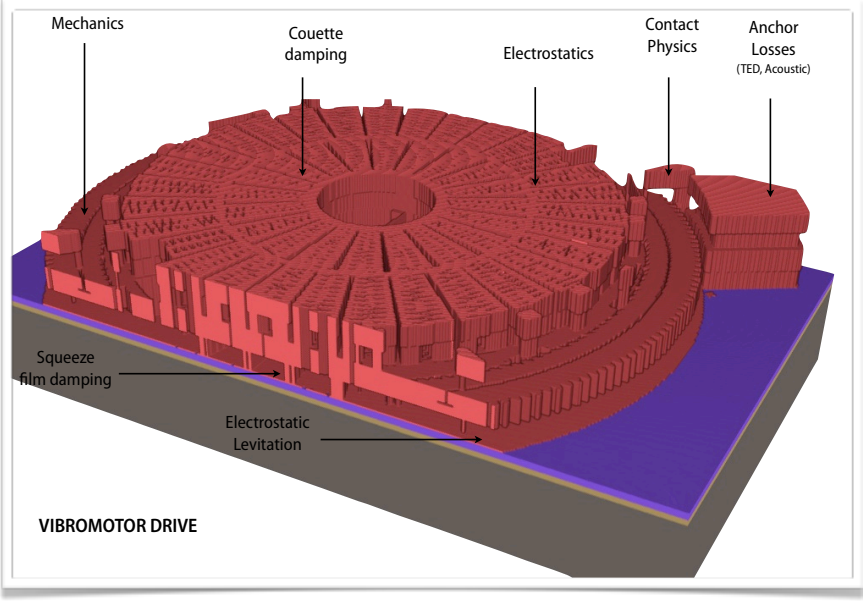
FEA/BEA tools are typically used to capture the multi-physical effects in MEMS devices

Layout-based design (Bottom-up design)

3D design, typically the entry mode for the mechanical designer, is still the most popular methodology for MEMS design. Originally pioneered by IntelliSense in the early 90's, this still remains the most popular methodology for MEMS design today.

Layout-based design combines the 2D mask layout with the process flow to create 3D solid models of the MEMS device. These solid models are discretized and analyzed using 3D Finite Element/Boundary Element Analysis (FEA/BEA) methods. Layout-based design has been tremendously successful in microstructure design because it combines design intent with manufacturing.

In addition, bottom-up design can fully capture the complex multi-physics inherent in MEMS devices.



System model extraction (SME)

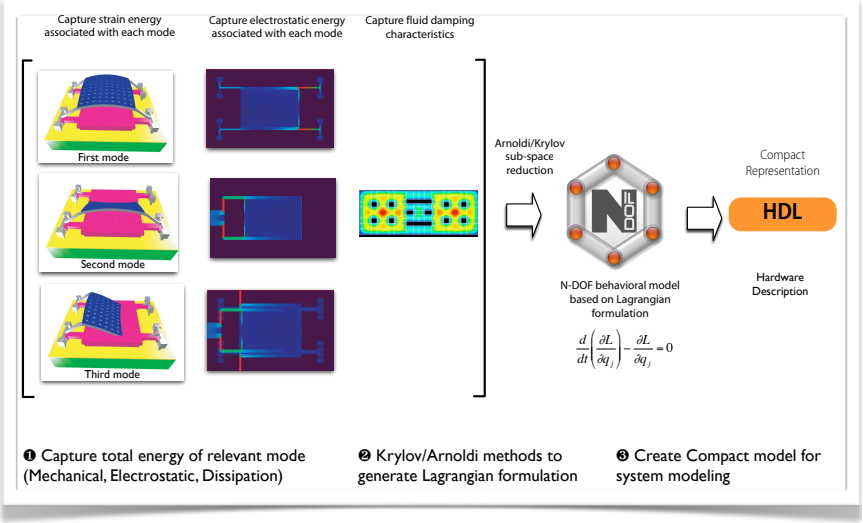
The layout-based discretized 3D models need to be converted into system models. Typical MEMS 3D models can contain between 100,000 – 1,000,000 degrees of freedom, while system simulators are not designed to handle such complex problems.

Many designers use lumped model approximations to represent the microstructure in system simulations. While these are sufficient for proof-of-concept analysis, they grossly simplify real-world effects such as etching effects, stresses in beams and suspensions, and levitation effects due to charge reflectance. For instance, sidewall angle due to etching can lead to large quadrature errors in inertial devices, residual stresses in beams can cause stiffening of beams, and levitation effects in comb drives can lead to lowered sensitivity of devices.

A new class of numerical algorithms based on Krylov/Arnoldi sub-space reduction techniques have been developed in the recent years to convert FEA models into arbitrary degree of freedom (NDOF) models. These algorithms are used to capture the total energy and energy dissipation in the system. Based on this, FEA/BEA models can be reduced to efficient compact system models that can be incorporated into system simulators. These compact system models, also known as Reduced Order Models (**ROMs**), can simulate the micro-device response to within 2-5% of the FEA/BEA model at a 100-1000X performance gain.

The advantage of using ROMs is that they accurately capture the device behavior across multiple energy domains (mechanical, thermal, electrostatics, fluidics, damping, etc). The **ROMs** can be typically exported into a variety of Hardware Description Languages (HDLs) for use with electrical or system simulators.

Figure 7 *(below): Methodology for efficient extraction of compact models. IntelliSuite creates Look Up Table based Lagrangian ROMs by capturing the energy in each of the physical domains (i.e. mechanical, electrostatic, fluidic, etc).*



Verification

Verification in MEMS is quite different from that in the IC world. The IC world typically uses Layout vs. Schematic (LVS) and Design Rule Check (DRC) techniques. While Design Rule Checks can be used in the MEMS world, support for curves, beziers, and all-angle geometries are needed. LVS provides little benefit to the MEMS designer due to the inherent 3D nature of the design.

Schematic vs 3D comparisons (**SV3D**) are needed to make sure that the schematic capture has been accurately translated into a 3D design. In MEMS design, verification is the process of comparing the results from the schematic-based model (top-down approach) with the results of the 3D-based approach (bottom-up approach). This typically involves benchmarking the schematic, 3D finite element and ROM results.

System simulation

Accurate system simulation can be performed using ROMs described in the previous section. However, compact models are not easily parameterized. While the process of creating a large number of compact models can be automated, it is time-consuming.

Another alternative is to use lumped parameter models. However, these models do not take into account process-related effects such as axial residual stresses, strain gradients, temperature coefficient issues, physical issues such as joule heating, squeeze film and Couette damping or package-level effects of die attach, plastic over-molding and non-uniform heating.

The designer is often faced with the choice of using low-fidelity lumped models which can be parameterized, or high-fidelity non-parameterized compact models. This makes the design optimization from a system standpoint a challenge.

Bottlenecks in current design flows

We can classify bottlenecks in MEMS design according the different stages of the design evolution. The bottlenecks in current MEMS design methodologies are summarized below.

Schematic and System level

- **Process information**: Ability to easily incorporate process tolerances and process corners. SPC information is often not available for Monte Carlo simulations.
- **High-fidelity models**: Ability to include high-fidelity models which fully capture multiphysics effects. Users need to capture effects of packaging, fluidic damping, temperature gradients and other non-idealities such as electrostatic gradients or stiction that can greatly influence the device performance.
- **Limited libraries**: Typical design libraries are limited in nature, and adding new components is a significant undertaking. While complex structures can be composed using basic shapes, schematic layout becomes an issue. Many MEMS schematic editors are little more than warmed-over IC design tools and are inefficient for MEMS design.
- **Ability to work with your favorite toolset**: Lack of true standards among EDA vendors has led to the creation of multiple quasi-standards, each of which has significant disadvantages. MEMS tools must support many of these quasi-standards including SPICE and its variants (PSPICE, HSPICE, ELDO), Verilog (-A, -AMS, SystemVerilog), VHDL-AMS (accounting for subtle but significant differences between tools) , and Matlab/Simulink.
- **Co-simulation with other system simulators**: While system-level simulators such as SYNPLE or SystemVision provide sophisticated functionality, there is a need for co-simulation along with other system simulators which may contain IP blocks or functionality not present in the tool of choice. The ability to mix system simulators such as SYNPLE with Simulink or Spectre will be extremely useful.

Physical level

- **Layout tools**: Popular layout tools like Virtuoso or L-Edit were originally developed for the IC world. Other tools such as AutoCAD were developed for architectural and mechanical drawing and are a bear to use for mask layout. Beziers, splines, and smooth transitions (essential for minimizing stresses) are often absent or an afterthought in MEMS layout editors.
- **High quality layout automation**: While schematic to mask synthesis exists in various tools, the resultant layouts are not production ready. Features such as smooth transitions, stress relief structures, release hole patterns, dimples and other secondary features need to be manually added to the layouts. This is often very time-consuming.
- **Geometry manipulation and meshing**: Design analysts spend a significant amount of time manipulating design geometries and meshing structures. Most MEMS design tools require manually partitioning 3D geometry into mesh-able regions. While many tools provide automated tetrahedral meshes, they are sub-optimal for MEMS

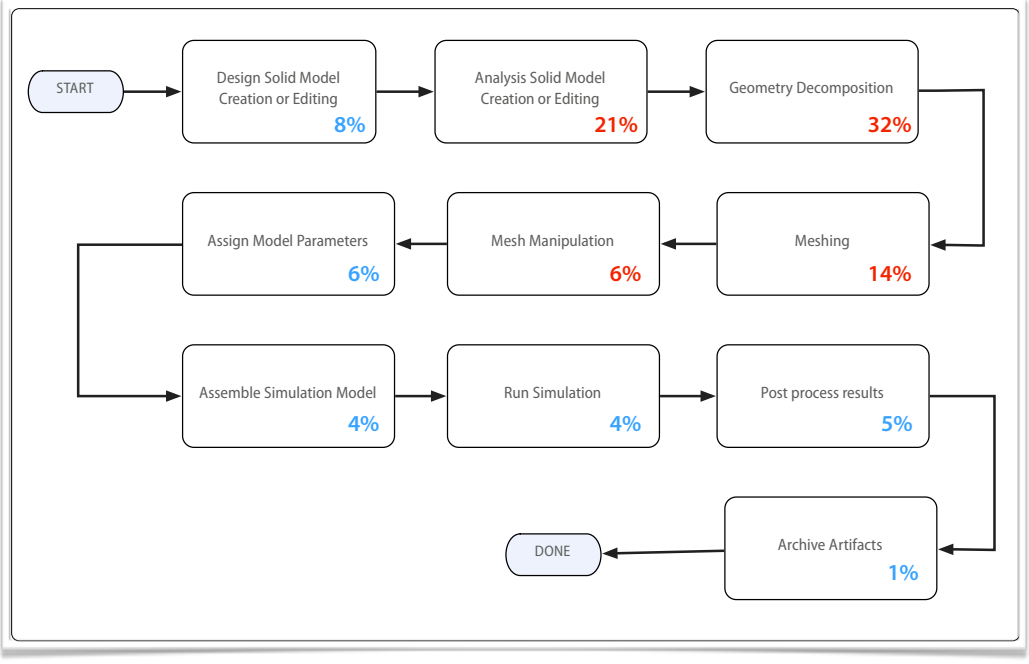


Figure 8 : *Design through analysis man hours spent (not CPU hours). A typical 10 step design through analysis cycle (excluding iterations) is shown. A staggering 73% of time is spent in geometry manipulation for meshing. [Courtesy: Matt Staten, Computing and Modeling Dept, Sandia National Labs]*

design. In the words of a Sandia Labs design analyst, "*The only people who use tets are those who don't care about their answers*".

Hexahedral meshes are ideally used for MEMS. The automatic generation of hex meshes has been the holy grail of the meshing community and is still a few years away.

- **Parametric meshing**: Any parametric changes to the MEMS geometry such as changing a film thickness or electrode gap requires a complete re-meshing of the structure. Parametric meshing and mesh morphing technologies are relatively new and are just making their way into MEMS design tools.
- **Incorporation of process corners into physical design:** As mentioned before, absence of reliable SPC data forces the designer to consider process corners based upon historical *estimates* of process tolerances. Users must manually configure their meshes for each of the process corners and run each process corner individually. This is highly time-consuming.

Process level

- **Process flow modeling**: Process engineers still spend a significant amount of time hand-drawing process flows in Powerpoint, Illustrator or some such tool. Any change in the process flow requires starting afresh in compiling the flow diagrams. While 3D process visualization and virtual prototyping was introduced by IntelliSense in 1995, full 3D visualization is time-consuming for large MEMS devices. There is a need to obtain 2D cross sections of custom process flows with minimal computing overhead. Better yet, automatic assembly of Powerpoint presentations would greatly simplify the process flow modeling.
- **Integrated cost and economics modeling**: Cost and economics are often an afterthought during the design process. Any changes to the design, process, or package configurations requires re-running Excel spreadsheets. Trade-offs between various configurations become difficult to envision without years of expertise. At present, design and process engineers have little or no visibility into the cost equation. Empowering engineers to make

economically sound decisions can go a long way in squeezing gross margins out of the product.

- **Deep Silicon Etch Simulations**: Deep Reactive Ion Etching (DRIE) is here to become the main stay of MEMS process technology. First generation DRIE simulation tools such as RECIPE and RECIPE3D can be used to fine tune sidewall angle of structures locally. Manual mask corrections need to be applied to ensure uniform etching across the die. Next generation tools, similar to optical proximity correction tools for lithography, are needed to automatically correct the masks to ensure uniform local etching of devices.

- **Incorporating accurate process details into meshes:** While tools like FABViewer™ and MEMulator™ can produce realistic device renderings, FEA meshing is often based upon idealized geometries rather than true geometries. Better meshing algorithms are needed to automatically create realistic meshes that are efficient to use in FEA simulations.

Structural level (3D simulation)

- **Enhanced ROMs**: System model extraction techniques have improved over the years from simple linear macromodels to accurate non-linear reduced order models (ROMs) that can accurately capture stress stiffening, electrostatic spring softening, and fluid damping. With the advent of wafer-level packaging and demand for low-profile MEMS for mobile applications, more and more of the packaging functionality is being subsumed into the MEMS. Packaging effects like temperature/stress effects and shunt capacitance calculations need to be automatically included into the reduced order models.

- **Parametric ROMs**: While the use of high fidelity ROMs in system simulation has gained adoption, ROMs suffer from the disadvantage of being tied to the original geometry. In a sense they are black box models. Users may prefer to have control over some of the device parameters, such as material thickness or electrode separations, for system-level optimization scenarios. This necessitates the creation of parametric ROMs. Parametric ROMs can be derived using Latin Hyperspace (LHS) based design exploration

followed by automatic fitting into a response surface for use in system simulators.

Synthesis and Optimization tools

- **Optimization tools:** While most CAD/EDA tools provide links to third-party optimization tools such as ModeFrontier, iSight or ModelCenter, the adoption of these tools into the MEMS design flow is non-existent. Impediments include poor integration, a steep learning curve, and the lack of optimization training in the MEMS industry. Many of these impediments can be solved by tightly integrating these tools into the design workflow and significantly simplifying the optimization setup.

IntelliSense's Design Methodology

IntelliSense's software architecture is based upon a unique combination of the best of bottom-up process-driven design and top-down synthesis. Top-down methodology allows you to quickly explore a wide range of design options, while bottom-up design provides the accuracy to produce first-time-right silicon.

IntelliSense gives you a distinctive methodology to tackle the conversion of product specifications and requirements into a working product. The accurate bottom-up process-driven design and top-down schematic-driven synthesis are combined to get you to your designs faster and with less process iterations.

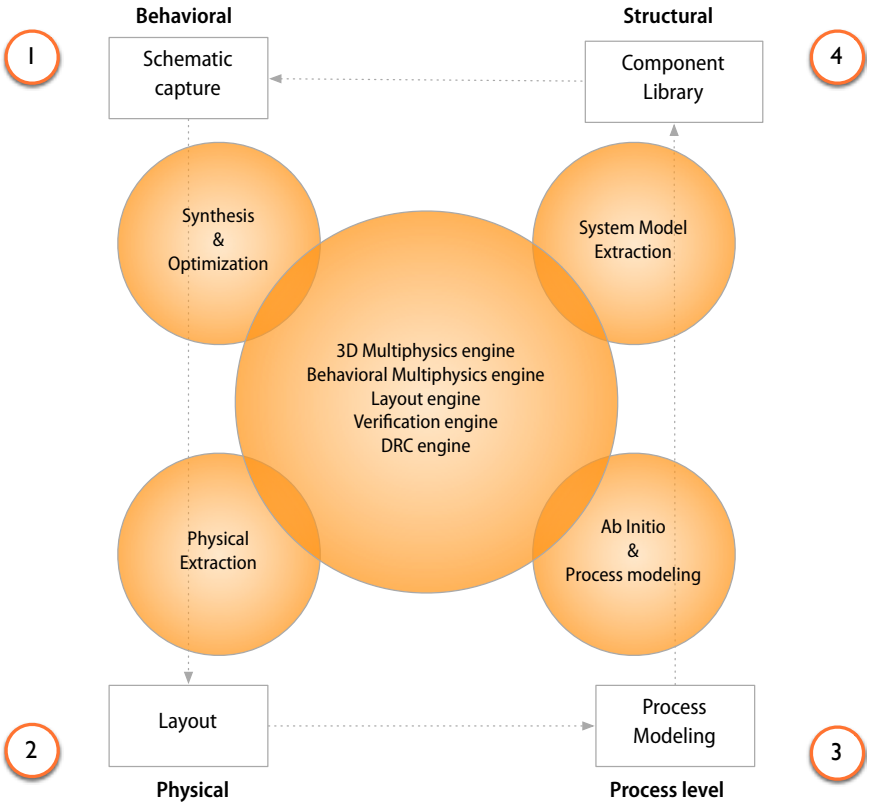


Figure 9 *: Design in IntelliSuite. IntelliSuite allows you to design and analyze your device at different levels. Core computational engines and databases combined with synthesis, optimization, process modeling, physical and system model extraction provide a friction-free and efficient workflow.*

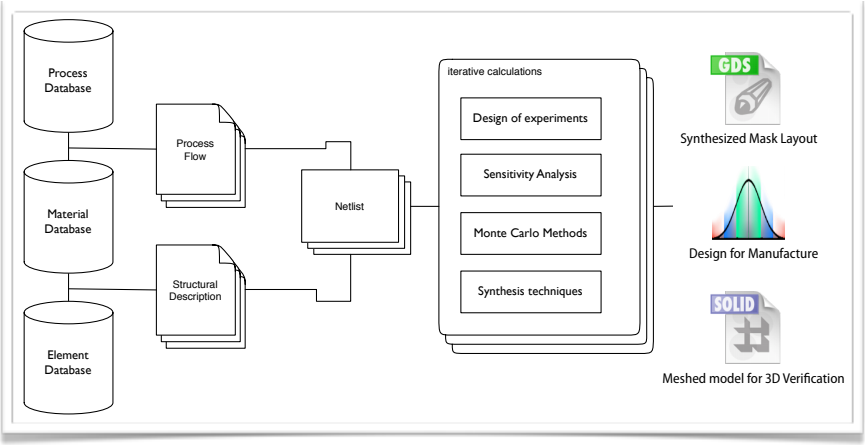
From the top down

State-of-the-art schematic capture and simulation tools allow you to take a hierarchical approach to the design space. SYNPLE provides a large multi-domain library of electrical, mechanical, thermal, digital and controls, and MEMS libraries. These elements may be combined in an effortless drag-and-drop fashion and then wired to create schematics of multi-scale, multi-domain systems. As a result, you can quickly survey a large design space before initiating a detailed analysis and verification process.

The top-down approach allows you to combine readily available component blocks into a *netlist*. Due to the simplified nature of the component models, users can perform device-level optimization using Design of Experiments (DoE), Robust Design or other techniques.

Users can start with component-based schematic capture and use optimization techniques to explore a vast design space. Built-in place and route algorithms can be then used to convert the schematic into a mask layout or an optimally meshed model ready for full 3D analysis.

Figure 10 *: Top-down modeling is fast but of lower fidelity. It can be used for rapid exploration of design space and optimizing the design for performance and manufacturability.*



One step at a time

IntelliSuite's bottom up architecture is based upon process elements — familiar process steps, such as photolithography, thin film deposition, and selective etching form the basis of understanding the final device geometries. By systematically building the prototype in IntelliSuite, you can identify costly process bugs before entering the fab, which ultimately saves time and money. The process steps, combined with the mask geometries, can be used to build the final virtual device (power users can also import 3D geometries from popular CAD programs). In addition, the analysis modules (fully-integrated thermo-electromechanical analysis, high-frequency electromagnetic analysis, micro-fluidics analysis) can be used to analyze the performance of MEMS models.

IntelliSuite features a comprehensive material and process database, allowing you to understand material properties like conductivity, film stresses and mechanical strength as a function of processing parameters. Subsequently, this enables you to produce more realistic models.

Etching has always been a bugbear in MEMS technology. We provide wet and dry etch simulators — a full anisotropic wet etch simulator for creating realistic models of your KOH, TMAH or EDP etches, and a dry etch simulator for simulating RIE/ICP and Bosch etch processes.

What's the bottom line? IntelliSuite allows you to use state-of-the-art model reduction techniques to automatically create compact system models from large finite element models.

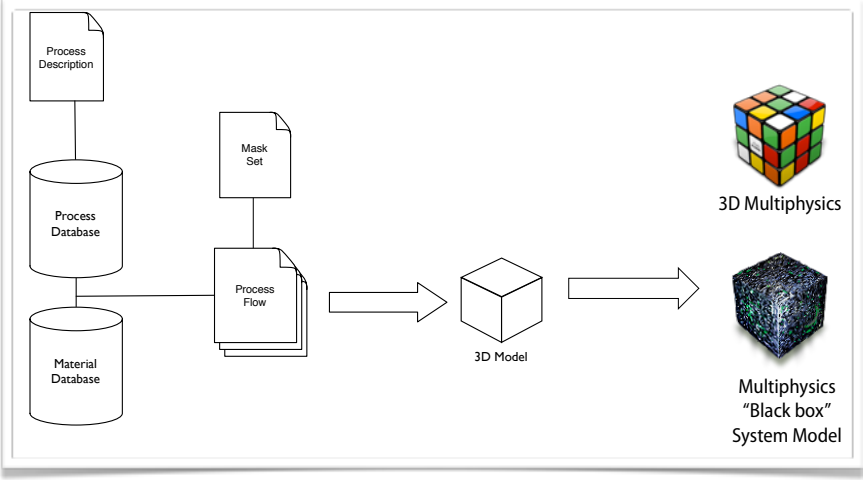


Figure 11: *Bottom-up modeling is accurate but slower. Use bottom-up modeling for accurately capturing the device behavior and encapsulating it into a black-box system model.*

Closing the loop

IntelliSuite offers you a number of tools to close the loop between top-down and bottom-up modeling. Synthesis and placement tools such as *MEMS-Synth* and *Hexpresso* can automatically transform the schematic into a ready-to-use layout or a meshed structure for FEA-BEA analysis. In addition, graphics tools allow you to visualize the results of schematic level analysis in 3D, the natural context for MEMS design.

Similarly, System Model Extraction (SME) tools based upon energy storage and dissipation in multiple physical domains can accurately capture the dynamics of the MEMS device. The Reduced Order Models from SME can capture all of the device and packaging effects. The derived ROMs can be directly used in schematic-level co-simulation with the electronics or alternately exported into popular Hardware Description Languages (HDLs) for use in simulators such as PSPICE, HSPICE, Cadence Virtuoso, Mathworks Simulink, and MentorGraphics SystemVision.

By presenting a uniform framework for simultaneous top-down and bottom-up methodologies and toolsets to easily switch between methodologies, IntelliSuite allows information capture from the entire design team.

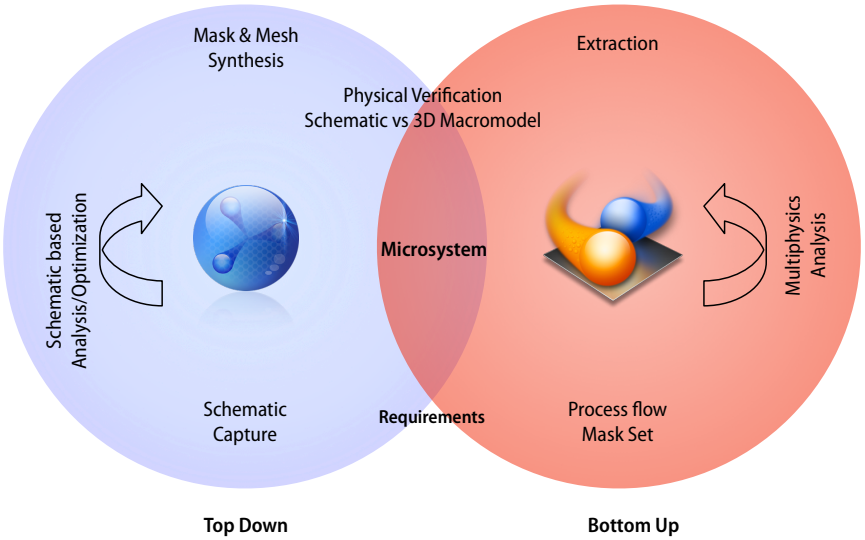


Figure 12: *IntelliSuite allows you to combine the best of top down and bottom-up methodology into an efficient workflow. Synthesis, optimization, and extraction tools are available to ensure an efficient workflow.*

Final thoughts

Living Design Environment

Ultimately, the development of a new MEMS product succeeds or fails based on the communication (or lack thereof) between different functional teams. MEMS teams require seamless communication across design, processing, packaging, controls, readout electronics and increasingly, software.

While point tools can capture parts of the information, an integrated approach is needed to maintain and evolve the design across the product life cycle.

IntelliSuite is designed as a tightly integrated environment that will link your entire MEMS organization together. Built to scale from a point tool to an organization-wide tool, IntelliSuite unifies various engineering and manufacturing tasks into a single living design environment.

Used by MEMS professionals worldwide for design, development and manufacturing of MEMS, IntelliSuite has firmly established itself as an industry standard tool. IntelliSense's tools are now used by large and small organizations in over 30 countries, including more than 60% of the top MEMS companies.